THESIS

STABILITY OF THIN-FILM CDTE SOLAR CELLS WITH VARIOUS BACK CONTACTS

Submitted by

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In partial fulfillment of the requirements

For the Degree of Master of Science

Colorado State University

Fort Collins, Colorado

Fall 2021

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ABSTRACT

STABILITY OF THIN-FILM CDTE SOLAR CELLS WITH VARIOUS BACK CONTACTS

With an increasing reliance on photovoltaic energy comes an ever-increasing demand to understand the mechanisms of failure which lead one to having an under-performing solar module. Recent technological advances have proven CdTe solar cells to be competitive with traditional Si, taking up 5% of the world solar market and reaching efficiency upwards of 22.1% for small area scale and 18.6% for module scale. This thesis explores various back-contact configurations to reduce the contact barrier height as well as how they hold up under accelerated lifetime testing.

Various degradation mechanisms, such as diffusion of species, drift within the built-in fields, and formations of various impurities/complexes on the surface and within the bulk were explored. The results of accelerated-lifetime experiments revealed the instability of devices with large amounts of Cu and those containing the colloidal Ni based paint solution as a metallic back contact. Sputtered films of nickel doped with vanadium (Ni:V) and chromium (Cr) demonstrated the capability to produce cells with efficiencies between 12-13% with fill factors up to 75%. Metallic bilayers containing a metallic cap of aluminum (Al) were then evaluated, demonstrating an increase in efficiency up to 15.1%. Buffer layers of NiO revealed the presence of a large back-contact barrier via the rollover effect in forward bias, leading to devices with efficiency of only 3%, but subsequent work revealed that by applying the NiO buffer prior to $CdCl_2$ passivation reduces the back barrier and produces cells with peak efficiency of 14.8%.

ACKNOWLEDGEMENTS

I would first like to thank Jim Sites for all of his guidance and mentorship in my research and in writing this thesis. I could not have done it without you.

I would also like to thank Jen Drayton for all of her assistance in fabricating and analyzing thousands of solar cells together. Additional thanks goes to my peers Alex Bothwell, Ramesh Pandey, Pascal Jundt, and Camden Kasik for always providing me with the help and encouragement I needed.

Final thanks goes to those from the Mechanical Engineering group, most importantly Walajabad Sampath. My research could not have been achieved without the work of Amit Munshi, Tushar Shimpi, Carey Reich, Adam Danielson, and Akash Shah. Thank you all for creating a successful and welcoming research environment.

DEDICATION

I would like to dedicate this thesis to my finance Sarina and cat Blizzard.

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Chapter 1

Introduction

This thesis will start by going over the motivation for renewable energies in today's world and establish why thin-film cadmium telluride (CdTe) is a strong candidate material for photovoltaics(PV). We will then cover the basics of semiconductor materials physics, from the definitions of materials based on their band structure to the way in which differing structures of the same materials can effect properties. This will lead into the building blocks of PV technology, the PN junction and it's electrical properties. From here we will review a brief history of CdTe and why it such a great PV material before discussing the fabrication procedures used to create solar cells at Colorado State University (CSU) and the analysis techniques to determine device properties. We will close the chapter by discussing accelerated lifetime testing (ALTing) as an engineering practice to determine defect propagation and general lifetimes of devices. Specific considerations for PV ALTing will be covered.

Chapter 2 covers the work done in developing new back contacts for thin-film CdTe at CSU. We will discuss the the issues present at the back contact, such as band misalignment and low carrier concentrations at the back surface. From here we will discuss changes which were performed at CSU to alter the back contact and the results of these changes. We will discuss the procedures for dialing in our absorber baseline, followed by investigations into differing Cu doping times, a look into the effects of sputtered metals in place of the typical colloidal nickle based spray paint back contact, and finally the use of semiconductor oxide layers as a back surface buffer.

Chapter 3 investigates the overall stability of thin-film CdTe solar cells fabricated with differing back contacts. The kinetics of defect propagation and the general physics of stability will be covered, looking into diffusion and drift of species under differing bias conditions and how these materials properties end up effecting the electrical properties of constitute devices through distortion in their JV curves. We will then discuss ALTing for thin-film CdTe and the types of information it is expected to provide. Results of ALTing various back contact configurations is ex-

plored, with emphasis on the stability of cells with differing Cu content and with sputtered metals in place of the Ni spray paint.

Chapter 4 will conclude with the overall findings of this research, with suggestions as to improved experiments and additional analytic methods to be performed in the future.

1.1 Photovoltaics

As the world continues to grow at an increasing rate, energy consumption too continues to grow. In 2019 there was a 2% increase in consumption to 600 exajoules [1]. Meanwhile, the effects of anthropomorphic climate change grow more pronounced each year, with the latest International Panel on Climate Change (IPCC) report showing unprecedented warming in the past decade, as is demonstrated in figure 1.1 [2]. Clearly there is a need, and indeed a demand, for better and cheaper renewable energies.

Renewable energies are defined as those energy sources which draw from naturally replenishing pools, such as wind, geothermal, and solar energies. Each of these resources is continuously available, albeit in a flow-limited setting. This differs from fossil fuel energy sources which are physically limited and require extensive work to extract from the Earth. [3]

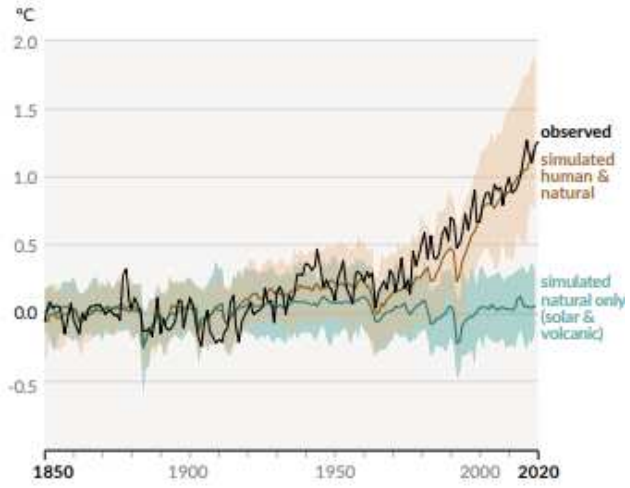

Figure 1.1: This graph shows the difference between simulated climate data with and without the human factor. A divergence towards hotter temperatures is seen near the turn of the 20th centure, indicating the impact of the industrial revolution on our climate. [2]

In the United States alone there has been a gradual shift from fossil fuels to renewable over the past century. While fossil fuel production saw an increase of 123%, from 32.55 quadrillion BTUs (quads) in 1950 to 75.65 quads in 2020, renewable sources saw a 295% increase in that same time from, from 2.98 quads in 1950 to 11.78 quads in 2020. Solar energy itself has seen a 2,011% increase in energy production between 1990 and 2020, demonstrating not just the demand, but availability of renewable energy sources. [4] As a matter of fact, solar energy is the most abundantly available source of renewable energy, easily supplying the entirety of world energy demands in as little as 115,00 square kilometers [5] - and this area will only decrease as PV technology advances. While we may never truly realize a world powered solely by PV, estimates show that renewables as a whole are on trend to become the largest source of energy consumption by 2050 [6].

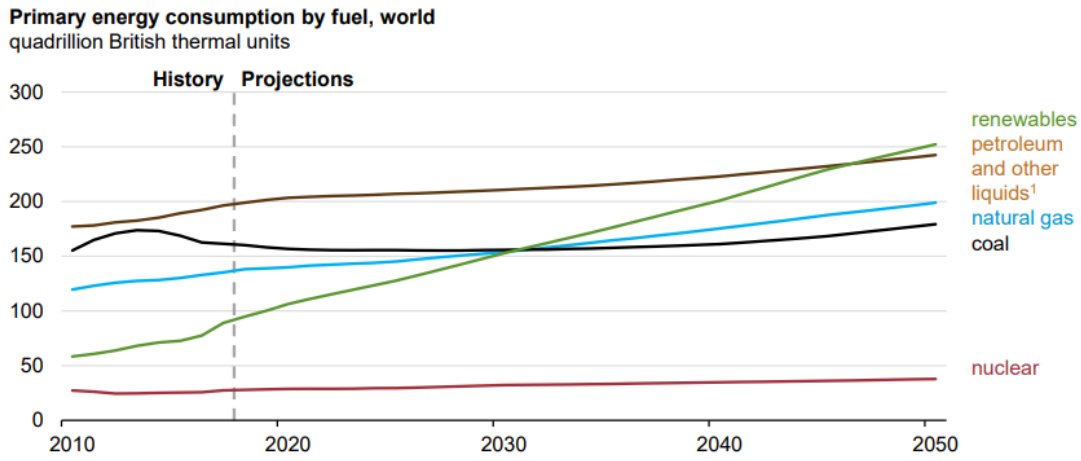

Figure 1.2: This graph shows the historical trend of energy production throughout the world up to 2019, with predictions showing renewable energy sources becoming the top producer by 2050. [6]

As this demand for renewable energies grows so too does the incentive to search for cheaper and better alternatives for PV energy production. The most common materials used in PV is silicon (Si), mainly because Si is one of the most abundant elements on earth. However, Si is a indirect bandgap material, requiring phonon assisted lattice transport for jumping from the valance to the conduction band. Additionally, Si has a rather low absorption coefficient over a majority of the visible range, show in Figure 1.3. This ends up requiring absorber layers in Si solar cells be on

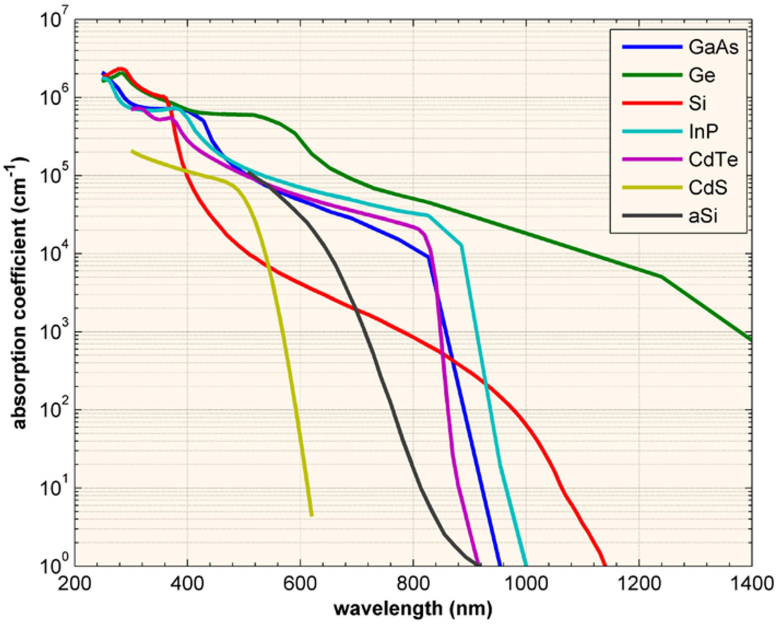

Figure 1.3: The low absorption coefficient for Si over the majority of the visible range means that we require a much thicker layers in order to ensure a majority of sunlight is absorbed. Note the CdTe curve in magenta

the order of 100s of microns thick in order to absorb a majority of incident sunlight. Additionally, Si processing requires extremely high temperatures and delicate techniques for developing single crystals. These drawbacks in Si have lead scientists to search for PV materials which can achieve the same results with less material and by use of quicker and cheaper fabrication processes. [7]

The thin-film revolution is a result of this, with direct bandgap semiconductors with near ideal band gaps being able to capture a majority of the terrestrial solar spectrum within microns of material, hundreds of times thinner than traditional Si PV.

In the next section we will cover the foundations of semiconductor physics which will lead us to an understanding of how PV devices are constructed from basic PN junctions up to entire PV stacks incorporating semiconductor-metal junctions as well.

1.1.1 Semiconductors

Semiconductors are ubiquitous in nearly all electrical devices in the modern world [8]. Having properties between that of metals and insulators, semiconductor properties are determined by

bother their elemental make up and their atomic structure. Semiconductors can be purely elemental, like the group IV elements Si and germanium (Ge), binary compounds, like the group II-VI CdTe or group III-V gallium arsenide (GaAs), and even high order compounds such as group I-III-VI copper indium gallium desellenide (CIGS). These differing semiconductors can be further divided between those which are crystalline or those which are polycrystalline.

In polycrystalline materials, grain boundaries (GB) form during crystal growth as crystals with differing orientation start to nucleate at different locations on the growth surface. As these differing crystal orientations meet, the atomic dislocations create the GBs which act as recombination centers.

Due to the inherent repeating lattice in crystalline and poly-crystalline materials, a periodic potential gives rise to energy bands [9]. As the temperature increases and electrons gain energy, their probability to occupy a free band state increases, as defined by the Fermi-Dirac distribution f(E):

$$f(E) = \frac{1}{e^{(E-E_F)/kT} + 1} \tag{1.1}$$

where E is the energy of the electron in a given state, k is the Boltzmann's constant, and T is the absolute temperature. These bands will be filled until they reach the Fermi Energy (E_F) which is that energy at which there is a 50% chance of an electron occupying said state at equilibrium [10]. When E=E_F, the exponential reduces to unity and we see that the probability is indeed 50%.

In the parlance of semiconductors, the bandgap (E_g) is defined by the energy difference between the valance (E_v) and conduction (E_c) bands. When there is energy incident on the semiconductor greater than that of the bandgap ($E \geq E_g$), an electron will be excited into the conduction band where it is then free to move and thus create a current. This leaves behind an empty energy state known as the hole. Holes are considered psuedo-particles in that they only exist in the absence of electrons and carry a charge equal and opposite to that of the electron.

The position of the Fermi level relative to the allowed bands will determine the conductivity, or lack thereof, inside a material. Metals are formed when the conduction and valance band overlap,

the Fermi level is found within an allowed state, easily contributing to current conduction. When the Fermi level resides between energy bands, and thus within the band gap of said material, this is known as a semiconductor. A material will become insulating once the bandgap is sufficiently large that it would require excessive energy for electron transport to occur over.

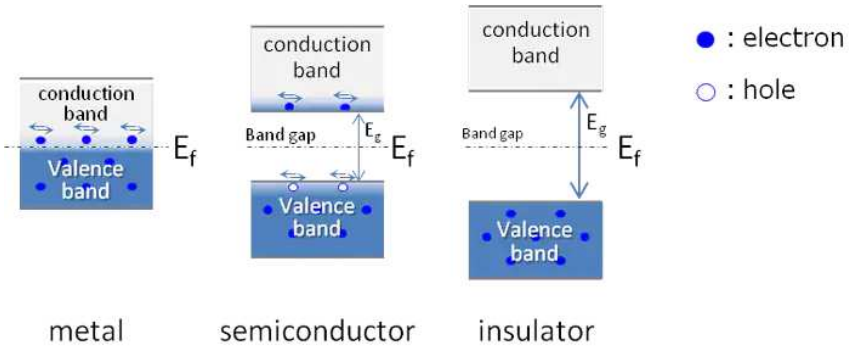

Figure 1.4: Band structures of insulators, semiconductors, and metals. [11]

The Fermi energy can be influenced by the addition of dopant impurities [10]. Dopants with a valency less than their constituent lattice will create acceptor energy states within a few kT of the valance band maximum, allowing electrons to easily be thermally excited out of the valance band and leaving behind a majority of holes. This will create an excessive positive charge, and thus we call this a p-type semiconductor.

Similarly, dopants with greater valency than that of their constitute lattice will form donor energy states within a few kT of their conduction band minimum and will allow electrons to be quickly thermally ionized into the conduction band, making electrons the majority carrier and shifting the Fermi energy to between the donor and conduction energy bands. This leaves an excessive negative charge and thus we call this a n-type semiconductor. Each type of semiconductor is shown in Figure 1.5.

The concentrations of electrons or holes within the semiconductor as given by

$$n = N_C e^{(E_F - E_C)/kT} \tag{1.2}$$

and

$$p = N_V e^{(E_V - E_F)/kT} \tag{1.3}$$

where N_C and N_V are the effective density of states for conduction and valance bands respectively and are given by

$$N_C = 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2} \tag{1.4}$$

and

$$N_V = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{3/2} \tag{1.5}$$

where $m_{n,p}^*$ are effective electron and hole masses, and h is Plank's constant.

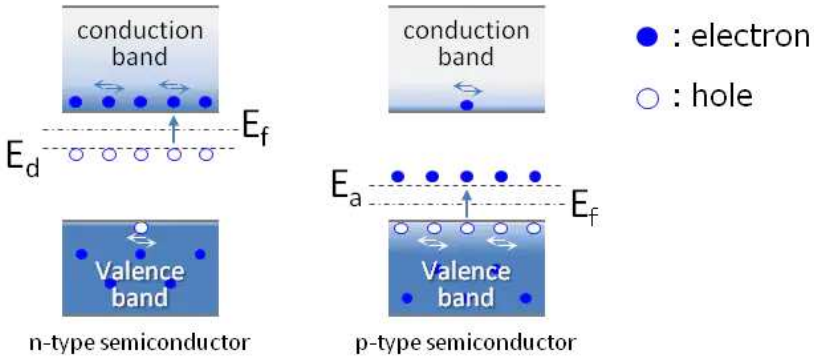

Figure 1.5: Band structures of n- and p- type semiconductors. [11]

1.1.2 PN junctions

Joining together a p-type and n-type semiconductor creates a PN junction, which is the foundation of most photovoltaic devices. The junction is considered a homojunction if both n- and p-type are the same materials or a heterojunction if the n- and p-type are different materials. As the two materials are joined, the excess electrons in the n-type material will diffuse toward the excess of holes in the p-type material, leaving behind naked ions with a net positive charge. This establishes

a built-in electric field pointing towards the p-type material, which grows in strength as the Fermi levels align at which point diffusion ceases, as shown below

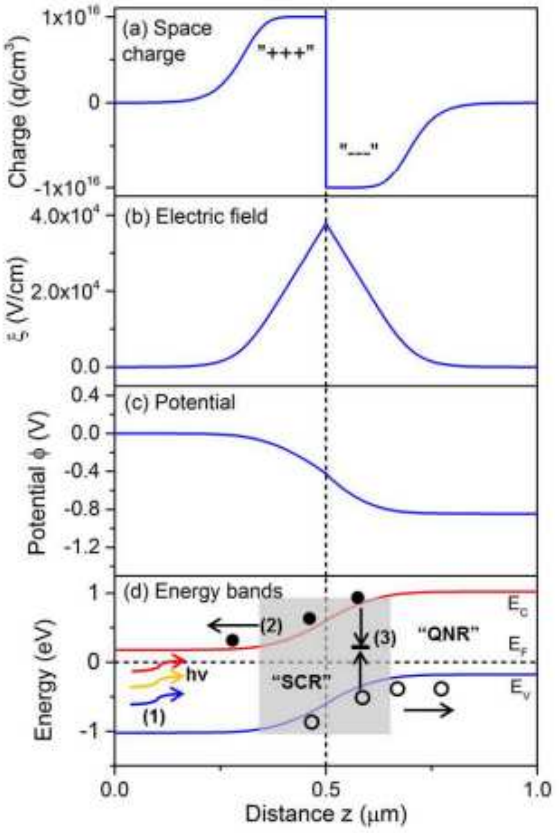

Figure 1.6: PN junction formation showing a) space charge distribution b) electric field distribution c) potential distribution d) band structure [12]

This abrupt change in dopant densities causes a gradual bending of the electronic bands as the Fermi levels align and creates what is known as the space charge region (SCR). Any charge carrier within the SCR will be quickly moved out by the electric field, ideally with conduction electrons going to the n-type and valency holes towards the p-type, where they will then be in a quasi-neutral region (QNR). This band bending creates a built-in potential defined as

$$V_{bi} = \frac{E_g}{q} - \phi_n - \phi_p \tag{1.6}$$

where ϕ_n = E_C - E_F, ϕ_p = E_F - E_V, and E_g=E_c-E_v is the band gap. This can be expressed differently when we consider the case of a non-degenerate semiconductor with

$$n_i^2 = e^{-E_g/kT} N_C N_V \tag{1.7}$$

such that

$$V_{bi} = \frac{kT}{q} \ln \frac{np}{n_i^2} \tag{1.8}$$

Applying an external bias across the PN junction causes extra charge carriers to be injected into the material, which creates a non-uniformity across the SCR and sets up quasi-Fermi levels for each carrier type. At forward bias, when a positive voltage is applied to the p-type region, the quasi-Fermi levels come together, resulting in the electric field strength reducing and allowing quick extraction of charges across the SCR, leading to an exponential increase in diffusion current with increased voltage. Reverse bias causes the quasi-Fermi levels to grow further apart, increase the electric field strength and decreases the diffusion current. This is all expressed by the diode equation as given by

$$J = J_0 \left[e^{\left(\frac{qV}{AkT}\right)} - 1 \right] \tag{1.9}$$

where k is the Boltzmann constant, T is absolute temperature, V is the applied voltage, A is the ideality factor and J_0 is the saturation current which occurs at large reverse bias. Under illumination, a photocurrent (J_{ph}) will be produced and acts as a current which flows against the current generated by a positive voltage injection. The total current under illumination is given by

$$J = J_0 \left[e^{\left(\frac{qV}{AkT}\right)} - 1 \right] - J_{ph} \tag{1.10}$$

The JV curve and PV working devices can also be modeled with an equivalent circuit as shown in Figure 1.7. The addition of the series resistor (R_S) accounts for general increases in resistivity

throughout the bulk or front and back contacts. Increasing R_S causes the JV curve to tend towards linearity, in line with Ohm's law V=IR. The shun resistance (R_{sh}) is a more complicated factor which accounts for imperfections within the manufacturing process, or imperfections which arise later, such as pinholes and scratches. Ideally, the shunt resistance (R_{sh}) would be infinite while the series resistance (R_s) would be zero.

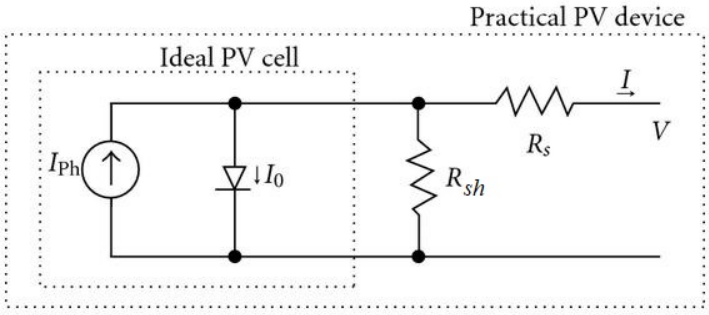

Figure 1.7: Equivalent circuit for PV devices showing the photodiode in the "ideal" square and then the real resistances which are experienced in the "practical device" square [13].

Taking into consideration the effect of these two resistors within the diode equation leads to

$$J = J_0 \left[e^{\left(\frac{q(V-JR_s)}{AkT}\right)} - 1 \right] + \frac{V + JR_s}{R_{sh} - J_{ph}} \tag{1.11}$$

This ideal current is reduced however through recombination of electrons and holes before they are able to reach their respective contacts. Recombination primarily occurs in three ways as shown in figure 1.8. Radiative recombination occurs as an electron from the conduction band falls back to the valance band, releasing a photon to conserve energy. Auger recombination occurs similarly to radiative recombination, where band to band recombination occurs, but the excess energy is imparted as kinetic energy to another particle within the band. Finally, trap/defect assisted recombination occurs as the electron and hole both fall into trap/defect states found in the forbidden band region, releasing a phonon to conserve energy. [9, 10]

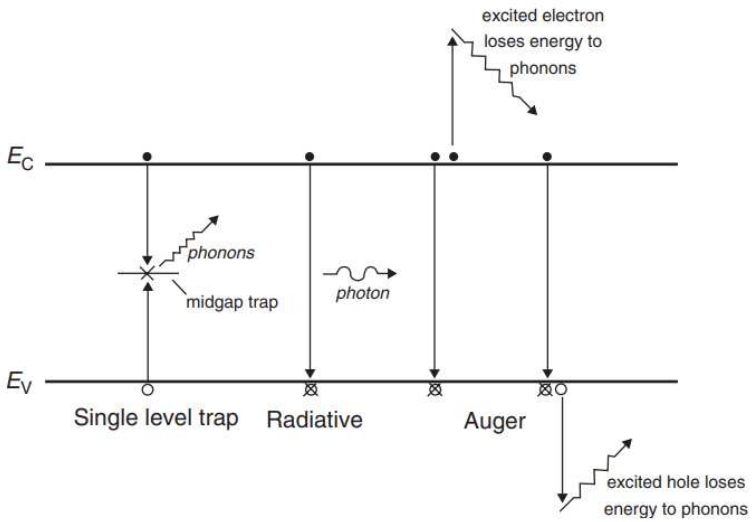

Figure 1.8: Different types of recombination events are shown here, including the propagation of auger recombination. [14]

1.1.3 Metal-Semiconductor junctions

The contact between metals and semiconductors (MS-junction) is essential for the operation of PV devices and has been studied extensively even before the advent of modern PV technology [15, 16]. The Fermi energy mismatch, or workfunction difference, between the metal and the semiconductor will determine the properties of this interface, as tabulated below.

	N-type	P-type
$\phi_M > \phi_S$	Rectifying	Ohmic
$\phi_M < \phi_S$	Ohmic	Rectifying
Barrier Height	$\phi_B = \phi_M - \chi$	$\phi_B = (E_g + \chi) - \phi_M$

The semiconductor has a workfunction defined as the summation of the electron affinity and the difference between the conduction band and Fermi band, $\phi_S = \chi + (E_c - E_F)$. An ideal Ohmic contact is created with p-type semiconductor when the metal work function is larger than that of the semiconductor. This allows electrons to flow from the semiconductor and into the metal, ultimately creating an upwards bending of the bands at the interface. As a result, the Fermi level

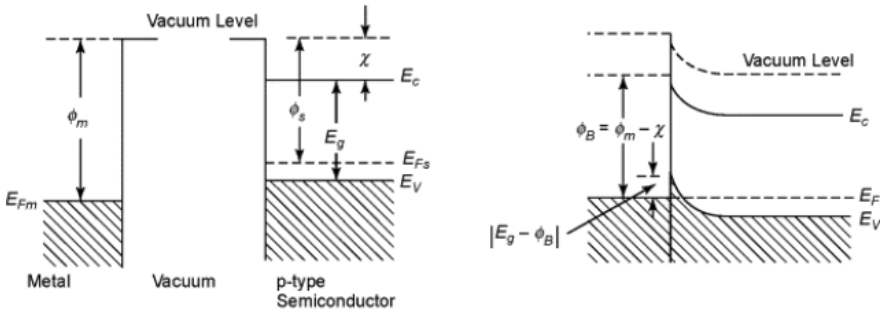

Figure 1.9: Before and after contact of a metal and p-type semiconductor with $\phi_M > \phi_S$. As contact is made, the Fermi level resides within the semiconductor valance band, leading to great hole conduction. [17]

resides within the valance band of the semiconductor at the interface, creating ohimc conduction of holes.

A rectifying contact occurs with a p-type semiconductor in contact with a metal with smaller work function than the semiconductor. As the metal and semiconductor are brought into contact, electrons will freely flow from the metal and into the semiconductor to lower their energy state until the Fermi levels equalize. The loss of electron generate a positive charge on the metal and forms a depletion region at the surface, which in turn forms a barrier for hole conduction. This barrier is given by

$$\Phi_B = (E_g + \chi) - \Phi_M \tag{1.12}$$

where E_g is the semiconductors bandgap, χ is the electron affinity of the semiconductor, and Φ_M is the metals work function. As we see from Figure 1.10 the Fermi level resides between the valance and conduction band, leaving us with the depletion region W and the Schottky barrier ϕ_B.

1.2 CdTe Solar Cells

In this thesis we will be focused solely on CdTe as our absorber material. CdTe is a II-VI compound semiconductor which forms a zincblend crystal structure and has a direct bandgap. This bandgap is well suited for the terrestrial solar spectrum, as shown in Figure 1.11 which when

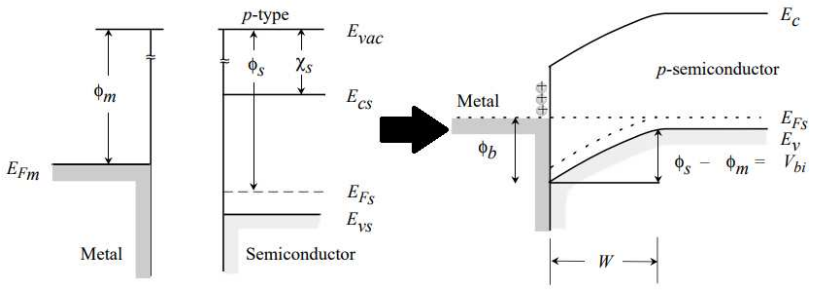

Figure 1.10: Before and after contact of a metal and semiconductor with $\phi_M < \phi_S$. As contact is made, the Fermi level still resides between the valance and conduction bands, causing resistance to hole conduction. [17]

coupled with a large absorption coefficient (>5E15 cm^{-1}) [18], enables CdTe films as thin as 2 microns to absorb upwards of 99% of photons with energy E > E_g.

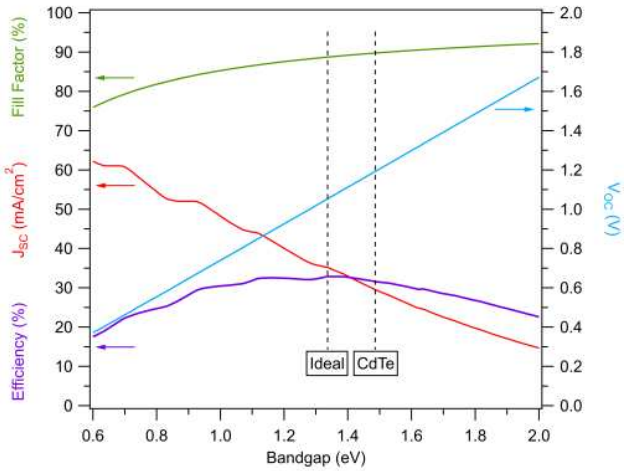

Figure 1.11: This graph shows the maximum theoretical short circuit current, open circuit voltage, fill factor, and resultant efficiency over a range of bandgap energies. Lines for CdTe and and ideal solar cell are referenced in black. [19]

CdTe has been an attractive material for PV applications since it was first shown that p/n-type doping could be achieved in 1954 [20], followed then by the demonstration that the conductivity could be controlled by varying the Cd-Te stoichiometry, with excess Cd giving n-type properties and excess Te providing p-type properties [21, 22]. The use of CdTe as an absorber layer was first proposed in 1956 [23], with much work beginning in the 1960's on applications of heterojunctions

using either p/n-type CdTe and efficiencies reaching upwards of 10% by the mid 1970's [24]. Since then, many advances have been made in the underlying physics and overall device structure leading to record efficiency of 22.1% and a market share of 5% [25, 26].

CdTe thin-films have been fabricated in a variety of methods, each with it's own advantages and drawbacks. A few examples of fabrication techniques are shown below. Within this work, close-space sublimation (CSS) is the chosen method of deposition. In CSS deposition, the CdTe source material dwells in a container which is equal in area to the superstrate for deposition, which is suspended directly above the source. A solid insulator separates the source material and the superstrate, allowing a temperate differential to form whereby the source material will sublimate and condense on the superstrate surface. The specific CSS processes used at CSU will be detailed in Section 1.3.3.

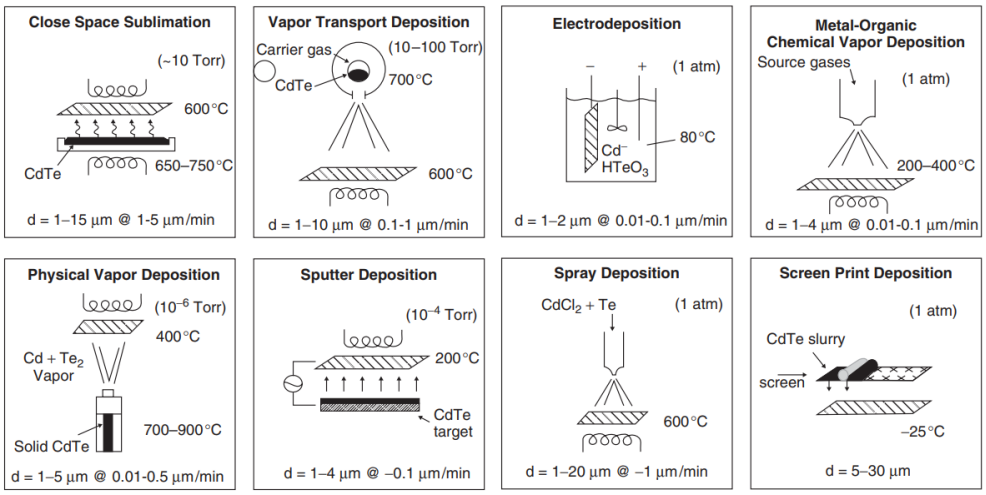

Figure 1.12: This graphic demonstrates 8 different fabrication techniques for depositing thin-film CdTe. The typical deposition thickness and deposition rates are listed at the bottom of each technique. CSS is one of the quickest methods for deposition. [27]

1.3 Thin-film CdTe

In this section we will review the typical structure for thin-film CdTe PV devices fabricated at CSU, as shown in Figure 1.13. We will examine in detail the materials used in each section of the solar cell and the processes used for fabricating said layers.

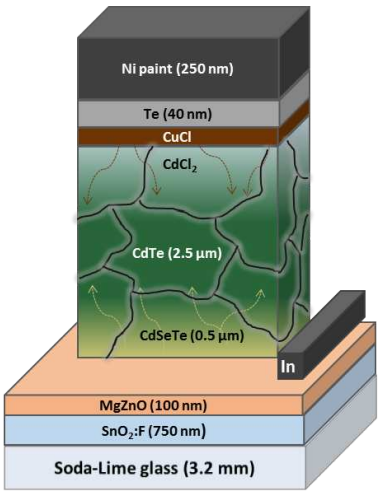

Figure 1.13: The initial structure for thin-film CdTe fabricated at CSU. Note the dashed arrows indicating diffusion of Se and Cu into the absorber during annealing; the large arrows indicating the direction light enters from; and the In solder bar used for making ohmic contact with the FTO.

1.3.1 Front contact

The superstrate of choice is TEC10 glass which contains a thin film of optically transparent flourine doped tin oxide (FTO). FTO operates as a front contact as it is a high bandgap oxide and thus optically transparent, as well as being highly conductive, making it a transparent conductive oxide (TCO). Most photogenerated carriers are created close to the front contact, where light is initial absorbed, thus it is critical for the front contact region to have a low recombination rate, yet be ohmic to electrons. This is typically done by deposition of an n-type semiconductor to create a built-in potential.

1.3.2 Emitter

An ideal emitter layer in thin-film CdTe would be highly n-doped, optically transparent, and easily fabricated. Historically, CdS has been used, however recent advances have identified Mg doped ZnO, MZO, to be an ideal candidate material. $Mg_xZn_{1-x}O$ (MZO) has a large bandgap (E_g > 3.3 eV) which allows a large portion of the solar spectrum to be transmitted while being energetically compatible with CdTe [28]. MZO has a tunable bandgap which can be modified by shifting the alloy's elemental content [29–31].

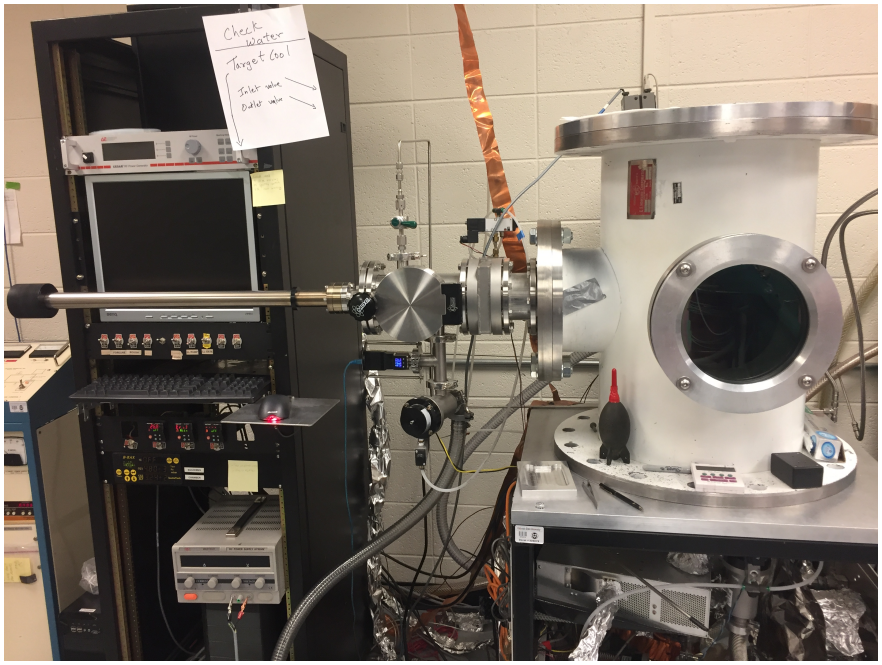

Figure 1.14: Tool used for deposition of MZO.

MZO is fabricated by RF sputtering of a ceramic MgO_xZnO_{1-x} target in argon using ht einstrument shown in . No additional heating is used during deposition. Our target thickness is a 100nm layer.

1.3.3 Absorber

As discussed in section Section 1.2, CdTe is an excellent choice for absorber material based on it's bandgap and absorption coefficient, among other ideal fabrication properties. However, as is seen in Figure 1.11 there is a slight boost in efficiency possible for bandgaps slightly lower than that of CdTe's. It has been demonstrated that CdTe can be alloyed with selenium (Se) to produce the tertiary compound $CdSe_xTe_{1-x}$ (CST) with a bangap of 1.4 eV [32]. This reduction in bandgap allows for larger wavelengths, and thus lower energy light, to be absorbed, thus increasing the output current. This increased current output more than compensates for the losses in fill factor and open circuit voltage.

Our structure uses a 0.5 micron thick layer of CST20, which is 20% CdSe by weight, deposited via CSS in the Advanced Research Deposition System (ARDS) shown in Figure 1.15. CST20

sources are held at 420°C top and 545 °C bottom. This is followed by 2.5 microns of CdTe to create an overall 3 micron thick graded absorber. CdTe source temperatures are held at 360 °C top and 555 °C bottom.

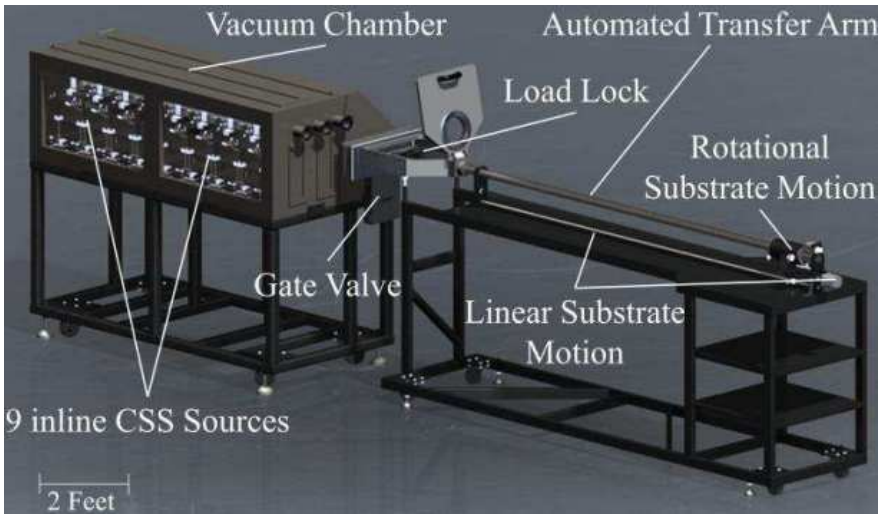

Figure 1.15: The Advanced Research Deposition Chamber (ARDS) is an inline CSS tool capable of producing 100s of solar cells in a day. The ARDS is where CST, Cdte, and $CdCl_2$ deposition occur.

It has been known for some time that more important than the deposition technique for the absorber itself is the post processing steps taken to passivate grain boundaries [33]. This passivation is needed as the grain boundaries within polycrystalline materials act as diffusional paths for dopants such as Cu, causing materials to be less stable. When passivized with Cl, stacking faults are reduced and grain sizes are increased and reoriented [34]. Additionally, the passivation creates an annealing stage for Se from the CST region to diffuse into the CdTe bulk and create a graded bandgap. Se diffusion and Cl migration to the boundaries is shown in

Chlorine passivation at CSU is achieved through CSS of $CdCl_2$ onto the CdTe free surface immediately following CdTe deposition without breaking vacuum. $CdCl_2$ source temperatures were 387 °C top and 440 °C bottom, with the shutter at 435 °C. After allowing the plate to rest and cool to room temperature, the residual $CdCl_2$ film is removed with a deinonized water rinse.

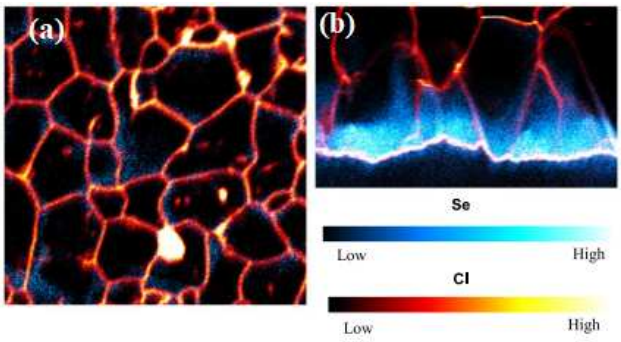

Figure 1.16: (a) SIM image of the back surface of a CST/CdTe solar cells (b) cross sectional view. We see the Cl has migrated to the GBs while Se has diffused slightly into the bulk. Trace amounts of Se are at the back surface, concentrated primarily along the GBs as well. [35]

1.3.4 Back contact

Unlike the near optimized front contact and absorber in thin-film CdTe, the back contact is plagued with problems. The back contact in the p-type CdTe solar cells serves the purpose of extracting holes out of the bulk to be used for work. An ideal material would be sturdy, inexpensive, easily manufactured and highly conductive. As we are concerned with the back side of our devices, optical transparency is not a limiting factor here. With this in mind, we will be considering the feasibility of using various back contacts based on the four factors listed previously.

The initial problem arises with forming an ohmic contact with the p-type CdTe. CdTe has a large electron affinity ($\chi = 4.28$ eV)V [18] which combines with it's bandgap to give us the required work function of $\Phi = 5.7$ eV. As such, a metal with a very large work function is required to avoid creation of a Schottky barrier [36]. A number of metals of interest are listed with work functions below [37]. As we see, metals with sufficient work function are nonexistent, and those with work functions which approach the required energy are scarce and expensive rare earth metals(Au and Pt). We thus expect a Schottky barrier to form at the back contact.

Metal	Work Function [eV]	Barrier height with p-CdTe [eV]
Pt	5.64	0.16
Au	5.47	0.33
Ni	5.22	0.58
Cr	4.50	1.3
Al	4.20	1.6

Various techniques are thus used to decrease this barrier height and help facilitate the conduction of holes into the back contact. The most common method of reducing the barrier height is through the introduction of copper which forms highly conductive acceptor defect Cu_xTe_{1-x} phases near the back surface. However, copper creates Cd substitution impurities (Cu_{Cd}) in addition to donor interstitial impurities (Cu_i), thus lowering the minority carrier concentration at the back surface [38, 39]. This fine balance between useful Cu surface states and harmful Cu complexes is the crux of back contact doping.

Cu is introduced to solar cells at CSU through CSS of CuCl in a vacuum in the system shown in Figure 1.17. Typical parameters are to preheat with sources at 330 C top and 330 C bottom, deposition sources at 170 C top and 190 C bottom, and finished with anneal sources at 200 C top and 200 C bottom.

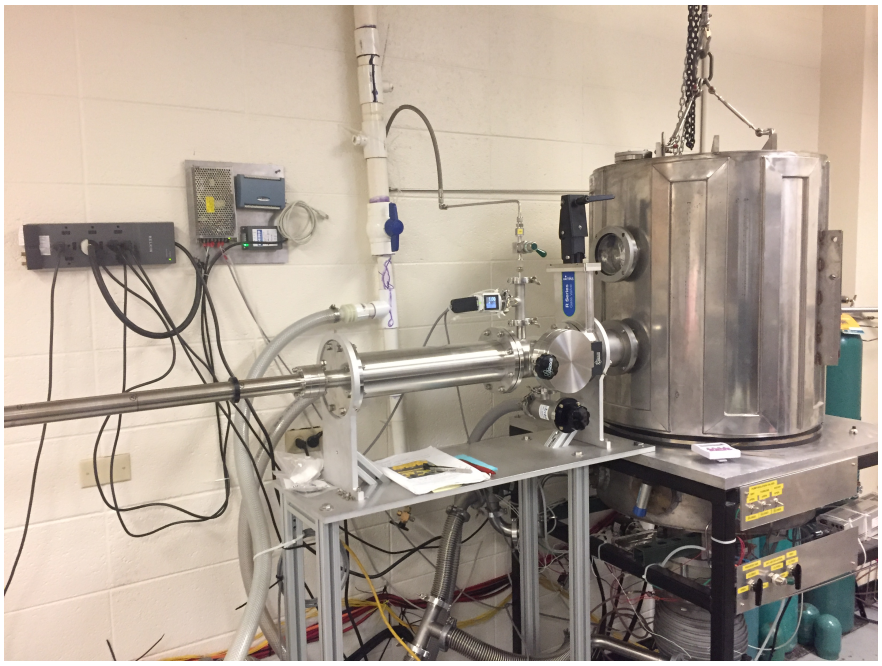

Figure 1.17: System used for deposition of Cu.

Besides increasing the carrier concentration at the back surface, general materials qualities improvements can be achieved for the free CdTe surface by changing the surface stoichiometry,

as discussed in Section 1.2. As we wish to achieve greater p-type conductivity, we deposit an additional 40nm of Te through thermal evaporation in vacuum.

The final step in producing the back contact is the deposition of a metallic contact. The typical method used at CSU is spray paint deposition of colloidal nickle, 841AR Super Shield Nickle Conductive Paint from MG Chemicals [40]. This paint based contact has worked to produce solar cells with efficiencies in the 16% range consistently, yet it is considered over-engineered and unneeded. The Ni paint dries into a very durable contact, which is nice but a moot point for devices which end up encapsulated under a secondary glass panel in the field. Following the metallic back contact deposition, plates are delineated into 25 devices each roughly 0.6 cm^2 in area each via sand blasting.

1.4 Characterization

In this section we will discuss the various analysis methods used to characterize thin-film solar cells at CSU. We will first discuss the background of each method and then the exact methodology and equipment used at CSU.

1.4.1 Current-Voltage Measurements

The definitive measurement for PV analysis, Current Density-Voltage (JV) measurements give information on the short-circuit current (Jsc), the open-circuit voltage (Voc), the current-density (JMP) and voltage (VMP) at the maximum power point (MPP) and the fill factor (FF), all of which come together to provide the operating efficiency (η) of the solar cell under measurement.

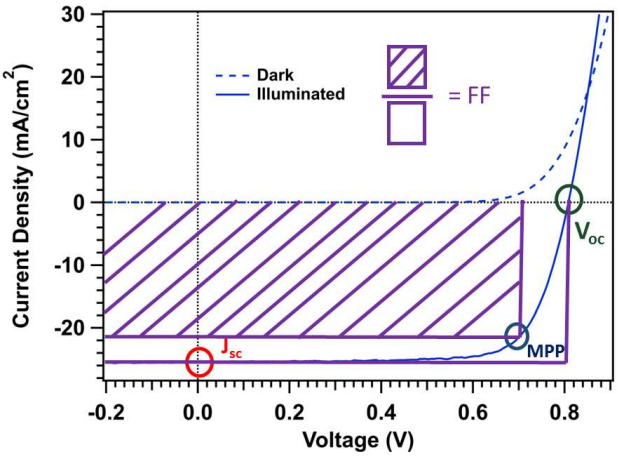

Figure 1.18: Example JV showing Jsc, Voc, MPP, and how they relate to fill factor.

The short circuit current is that current measured from the photovoltaic device under illumination with no potential bias applied and is less than ideal due to photon conversion losses. As there is no applied bias across the junction, any current measured is thus due purely to the photocurrent, as is seen from equation (1.10) when V=0.

The open circuit voltage is the potential which reduces the current to zero under illumination and is also less than the ideal Voc due to recombination. Again, from equation (1.10) when J=0 and solving for V we find

$$V_{OC} = \frac{AkT}{q} \ln \frac{J_{ph}}{J_0} \tag{1.13}$$

The fill factor is a materials parameter which relates the maximum power point to the product of the Jsc and Voc. Geometrically, the fill factor is the area of the largest rectangle to fit within the JV curve, according to the equation

$$FF = \frac{V_{MP} * J_{MP}}{V_{oc} * J_{sc}} = \frac{MPP}{V_{oc} * J_{sc}} \tag{1.14}$$

The total efficiency of the cell is the ratio of power in to power out, which can be related to the FF, Voc, and Jsc using the equation

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{oc} * J_{sc} * FF}{P_{in}} \tag{1.15}$$

JV is done under two conditions, when the cell in the dark and when the cell is exposed to light. The light curve is measured while the cell is under Air Mass 1.5 (AM1.5) intensity, which is the standard spectrum used for profiling PV performance for terrestrial applications and corresponds to a spectral intensity of 100 mW/cm^2.

JV measurements presented in this work were performed at the CSU photovoltaics laboratory inside a light-tight enclosure. Illumination was provided by a Solar Light Company AM1.5 simulator with a model XPS400 xenon lamp power supply. A Keithley 2401 sourcemeter was used to set a bias. The light intensity was adjusted to AM1.5 by measuring the current of a calibrated GaAs cell. JV data was collected with a four point probe and stored using LabView software.

1.4.2 Luminescence Imaging

In luminescence imaging we are interested in forcing the recombination of charge carries to create spontaneous emission which is measured using a variety of techniques. The two primary forms of luminescence imaging used is electroluminesence (EL) and spectral photoluminesence (Pl). EL creates spontaneous emission through electrical injection of charge carries via a strong electric field or large current, essentially forcing the PV cell to operate in reverse of its typical role and act as a light emitting diode (LED).

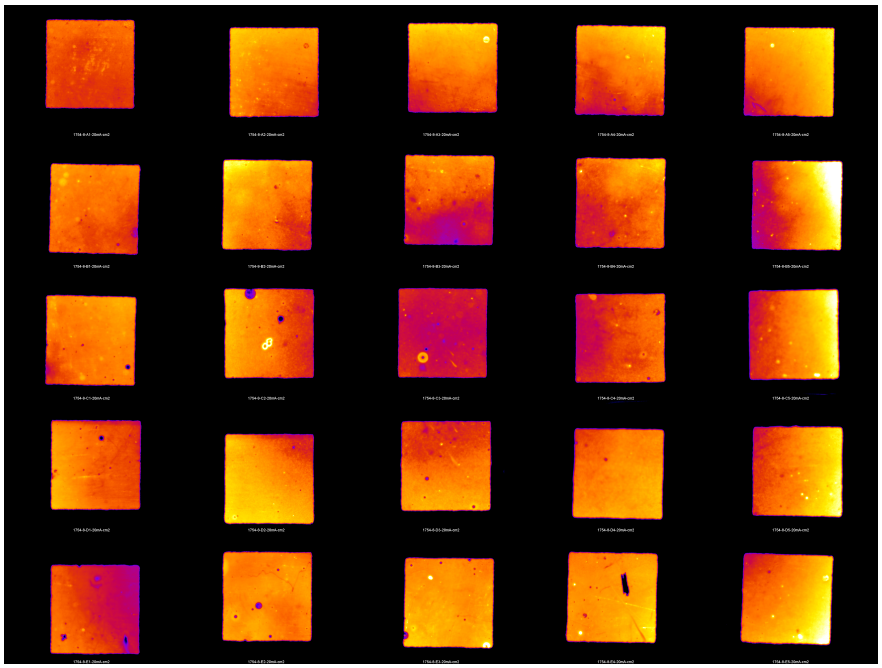

Figure 1.19: Example of Electroluminesence (EL) imaging across a full plate of 25 devices.

Within thin-film CdTe, radiative recombination of injected free carries occurs between the conduction band and the valance band during forward bias operation. However, a majority of recombination processes are non-radiative, resulting in the excess energy in the form of heat. The intensity of the EL image is proportional to the number of injected carriers, thus imaging is done at constant-current mode. Analysis of the EL image can be done either spacial, observing the changes in intensity across the face of the solar cell, or spectrally, where the spectrum of the emitted light is analyzed. The main mode of analysis at CSU is spacial analysis through use of the NIH program ImageJ.

Imaging is done with a Finger Lakes Instrumentation CCD camera attached to a gimble which can be moved for focusing as shown below. Emission from the device is achieved using an Agilent E3611A DC power supply at constant current mode, typically 20 mA/cm^2, with the current monitored by a Hewlett Packard 34401A multimeter.

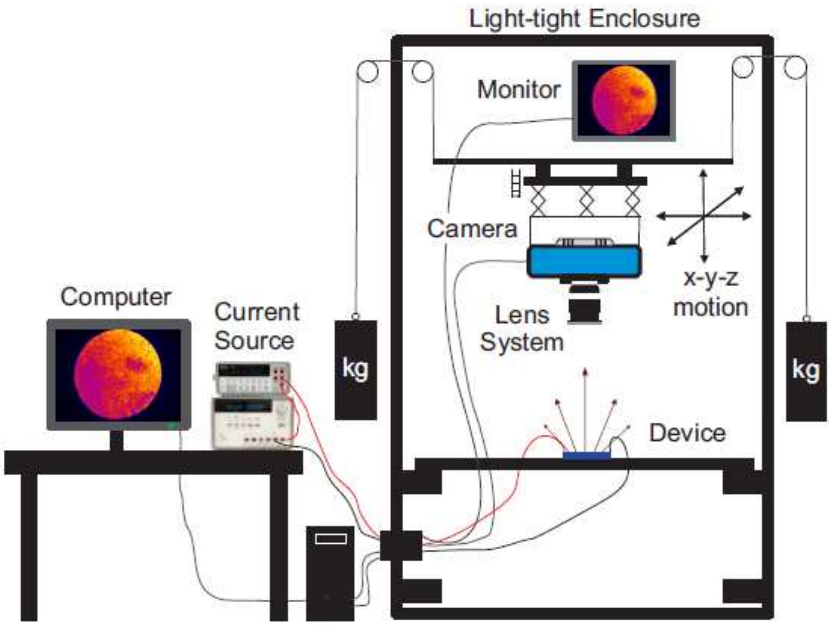

Figure 1.20: Schematic representation of the EL system at CSU.

PL is focused on the spectral analysis of the emitted light from the device resulting from photo induced radiative recombination. This spectral profile will consist of mainly band-to-band radiative recombination, in addition to conduction-band-to-acceptor-state, donor-state-to-valance-band, and donor-state-to-acceptor-state transitions. The resulting spectral image with be a broad Gaussian peaking at the band gap with a peak intensity proportional to the number of charge carries radiatively recombining across the bandgap. Other peaks within the PL spectrum are representative of other transition energies, with their peak intensities also correlating to the number of charge carries recombining across that transition state. The choice of probe is determined by the material you wish to probe, with larger wavelengths penetrating shallower depths.

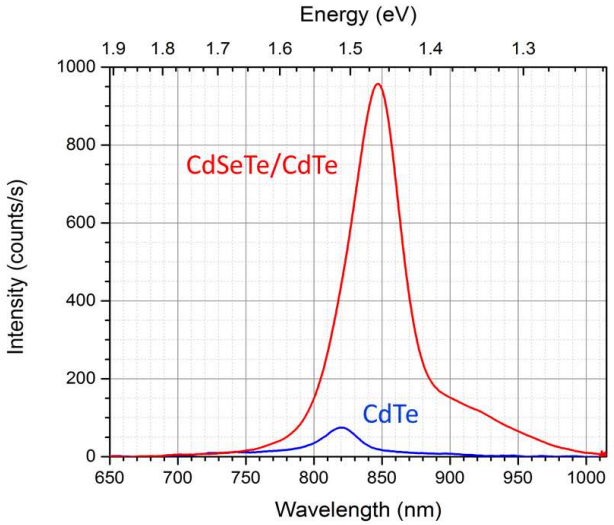

Figure 1.21: Example of a typical PL graph from CSU. Note the difference in bandgap, as given by peak location, for the CdTe absorber versus that with the graded CST20-CdTe absorber.

The PL system at CSU uses a ThorLabs Laser Diode Controller to drive a 520nm laser at 15mW, which strikes the cell surface using a set of mirrors enclosed in a light tight box. The light subsequently emitted from the cell surface is then directed into a fiber optic cable attached to an Ocean Optics IRRAD2000 spectrometer.

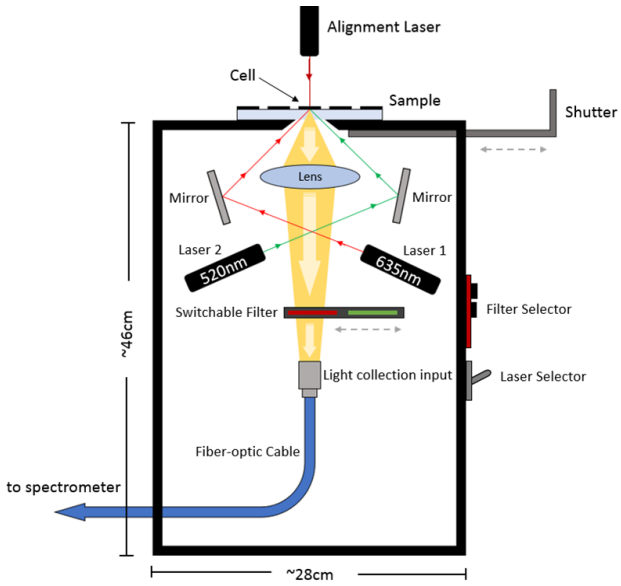

Figure 1.22: Schematic representation of the PL system used at CSU.

1.5 Accelerated Stress

One of the benchmarks of a well behaved device is it's stability under stressed conditions. Ideally, a solar cell will retain it's performance after being exposed to a variety of stressing environments, such as extreme temperature fluctuations, high humidities, high impacts, etc... Typical modern systems will offer warranties guaranteeing a minimum of 80% power performance retention after 25 years of operation [41]. This is not always the case tho, with some modules showing stability with virtually no appreciable loss in efficiency, while some modules will fail within the first year of deployment and still others will actually increase in efficiency during their tenure. This large range of degradation rates is due to the large range of factors effecting module degradation, from initial materials quality and fabrication processes, to the environmental conditions and power demands placed on modules in field. Clearly it is a rather complex matrix of factors which account for observed degradation. In order to better understand how each individual factor impacts the propagation of defects and overall stability of cells, we must isolate specific stressing mechanisms and elucidate the affect each has, looking for overlapping and possibly co-contributing factors which lead to the overall degradation.

Considering the rapid development of CdTe modules on a global scale, there is a great need for understanding these degradation methods quicker than traditional field degradation studies can achieve. For this reason, accelerated stress testing is an attractive alternative to traditional degradation studies which can help identify degradation pathways exponentially quicker than could be otherwise.

Within this work, the performance of various back contact configurations will be evaluated through Accelerated Lifetime Testing (ALTing), in which our PV devices are exposed to elevated temperatures for an extended time under various illuminations. The aim of this testing is not only to determine the long term stability and performance of these various back contacts, but to better understand the fundamental physics which dictate their degradation through diffusion of ions and phase changes within the materials. Differing avenues of degradation will be explored by examining JV curves and EL images of devices with differing stressing conditions.

Chapter 2

Engineering the Back Contact

2.1 Motivation

While the absorber in CdTe PV has nearly been optimized, the back contact still poses a challenge in achieving peak efficiency. This challenge arises mainly band misalignment at the back contact, a result of the rather large CdTe electron affinity (4,5 eV) and the low p-type carrier density (10^{13-14} cm^{-3}) which causes problems with band alignment and providing carriers to penetrate energy barriers. In order to create an Ohmic contact we will require a metal with either a sufficiently high work function, (>5.7 eV) or one which has a narrow enough Schottky barrier to allow tunneling between the CdTe and metal contact. These problems are worked around by creating a tellurium rich surface, either by etching of the absorber or by deposition of a thin Te film, and by doping the absorber back surface to increase carrier concentration.

Doping the back interface of the CdTe absorber is one way to create a semi-ohmic contact. Copper is an excellent dopant which increases the p-type carrier density to the order of 10^{15}, but due to the high mobility of copper inside of CdTe, Cu ions tend to diffuse out of the junction region and into the bulk of the device over time.

2.2 Analysis of changes to the back contact

In this section we will review how changes to the back contact structure effect the performance and quality of devices. We will begin by establishing an absorber baseline through differing chlorine passivation treatment, then discuss changes to the amount of Cu doping and annealing time following doping. We will then move into the results of using various sputtered metallic back contacts, examining Ni:V, Cr, and metallic bilayers of Cr+Al. We will conclude with preliminary experiments in using a metal-oxide buffer layer, NiO, in front of the back metallic contact.

2.2.1 Establishing absorber baseline

To begin evaluating how our performances changes with a changing back contact we must establish a baseline to compare against. This baseline experiment was meant to determine the optimal absorber for our initial back contact of nickle based paint in conjunction with a thin tellurium buffer layer and a copper doped absorber. The structure for this baseline consists of TEC10/MZO/CST20/CdTe:Cu/Te/Ni paint as shown in 1.13.

Our absorber consists of a 3 micron thick graded semiconductor bi-layer of 0.5 microns CST20 and 2.5 microns of CdTe. One of the most important steps in CdTe fabrication is the chlorine passivation step, in which the grain boundaries present within the poly-crystalline bulk absorber become occupied by molecular chlorine to prevent trap states from appearing within the full device. As this is a new absorber structure, it is worth experimenting with various chlorine deposition and annealing times to determine optimal film quality. Two parameters were varied, first the time which the plate dwells within a $CdCl_2$ rich environment, and second the time which the plate sits in an inert chamber to anneal.

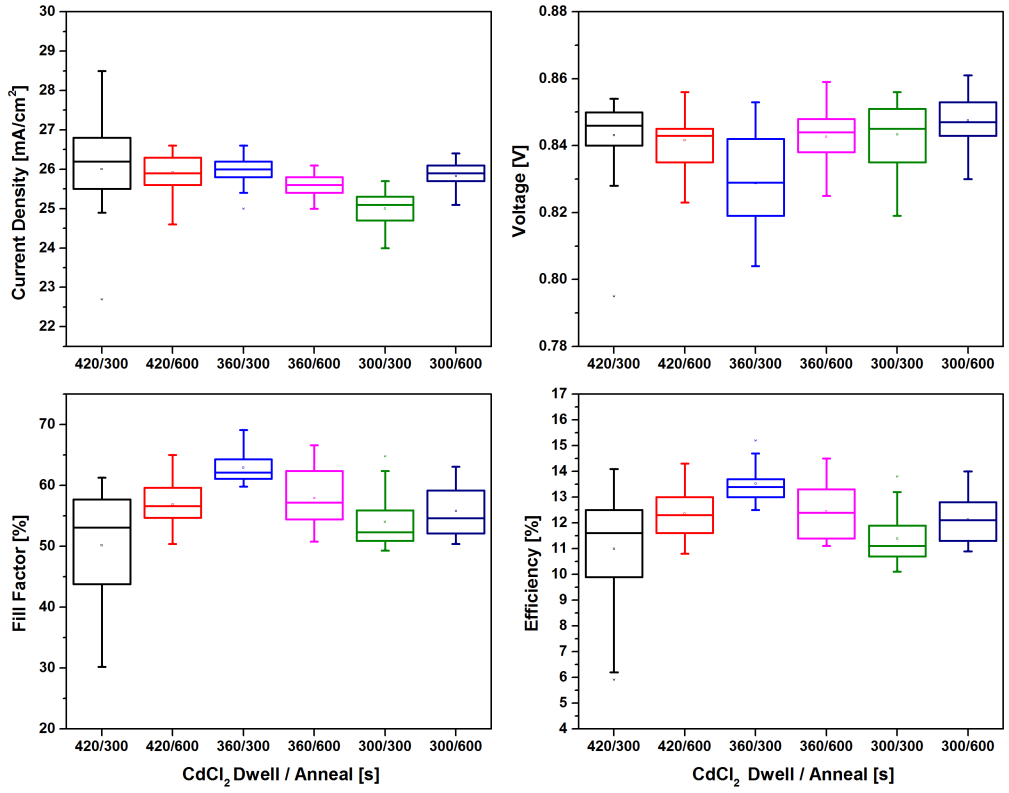

Figure 2.1: Box plots demonstrate the peak in performance for devices which received 360s of $CdCl_2$ and were anneal for 300 or 600 seconds.

Table 2.1: Best performing devices with various chlorine deposition times

CdCl2 dwell time [s]	Anneal time [s]	Voc [mV]	Jsc [mA/cm^2]	FF [%]	Eff [%]
420	300	842	28.5	59.1	14.1
420	600	843	26.4	65	14.3
360	300	842	26.2	69.1	15.2
360	600	854	25.6	66.6	14.5
300	300	854	25	64.8	13.8
300	600	856	26.1	63.1	14

We see a peak in performance when devices dwell within the $CdCl_2$ chamber for 360 seconds, which can be attributed to a greater fill factor for those devices, as is reflected in the box plots

presented in 2.1. However, PL shows a greater response for cells which received only 300 seconds of $CdCl_2$. EL additionally reveals a greater uniformity across the surfaces of cells with the shorter $CdCl_2$ treatment as well. This indicates the need to reexamine the difference between cells with a shorter $CdCl_2$ treatment and longer anneal time vs those with a longer $CdCl_2$ treatment and shorter anneal time in order to truly dial in the proper baseline.

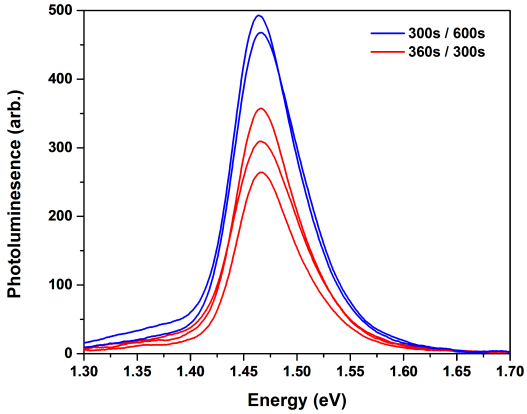

Figure 2.2: PL signal is stronger for devices which received only 300s of CdCl and were annealed for 600s.

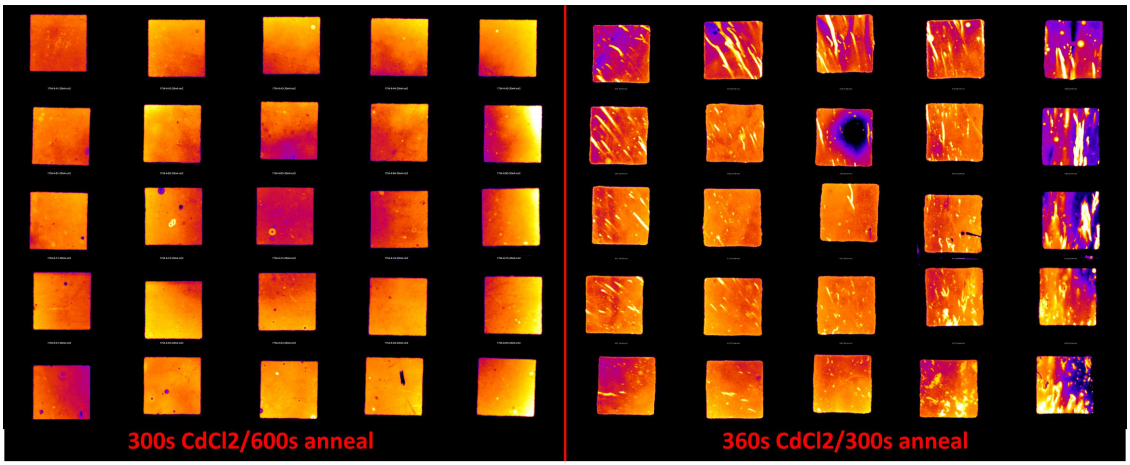

Figure 2.3: These two images compare the EL surface luminosity across a full plate with two differing passivation treatments. We see that the longer $CdCl_2$ deposition with a shorter anneal is less uniform.

To avoid any differences in absorber quality throughout the fabrication day, device production was alternated between the longer and shorter $CdCl_2$ processes. Evaluation of the efficiency of 75 cells across 6 plates reveals that the shorter CdCl passivation time with a longer anneal time produces more consistent results. On average we have 13.1±0.94% efficiency for the 300s/600s treatment versus 12.3±2.04% efficiency for the 360s/300s treatment.

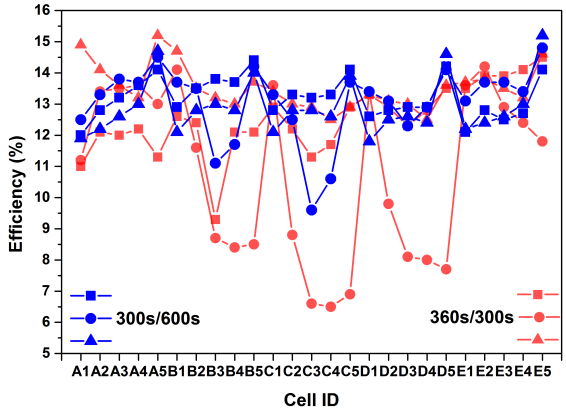

Figure 2.4: This graph shows the efficiency graphed across the full plate for 6 plates comprising 150 solar cells.

2.2.2 Varying the copper doping

Now with an optimized absorber process, we can begin evaluating changes to the back contact process/ The first step towards optimizing the back contact is through varying the amount of copper deposited into the back surface of the CdTe bulk while retaining the rest of the typical back contact structure as outlined in 1.3.4. The amount of copper deposited is controlled by leaving the plate to dwell within the CuCl chamber for various durations. We first look at dwell times centered around 5 minutes, with best results shown in the table below.

In figure 2.5 we see a general trend of increasing performance with increasing copper doping, which is expected based on our understanding of coping doping aiding in increased carrier concentration. This increased performance is mainly attributed to increased short circuit current, however this plateaus at 5 minutes. It should also be noted that the spread is tighter for greater doping times.

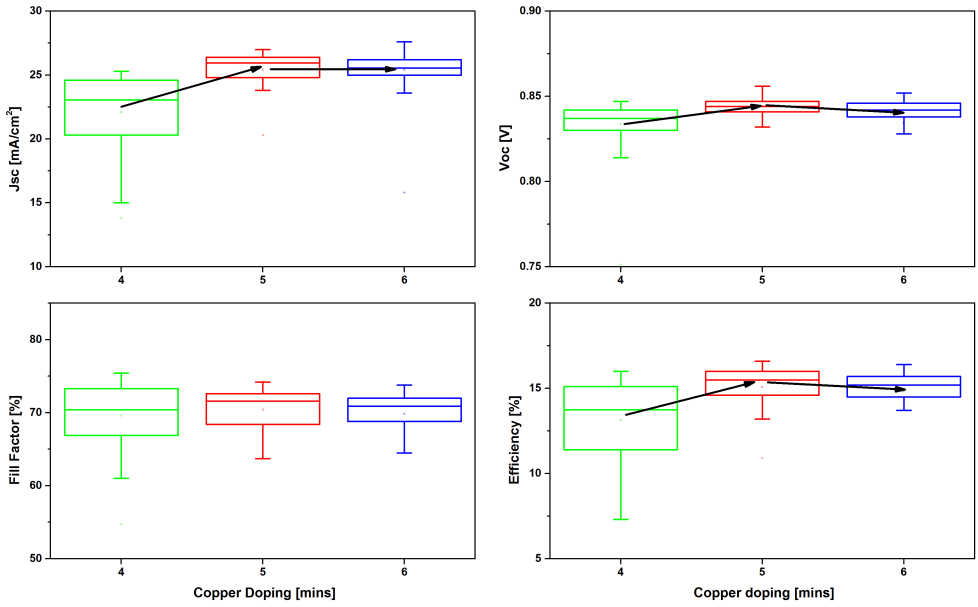

Figure 2.5: Example JV curves and box plots of 50 devices each for 4, 5, and 6 minutes of copper doping. Note the increase in short circuit current as copper is increased until plateauing at 5 mins, which results in a slight lowering of the performance for greater doping times.

With this apparent plateauing at 5 minutes as seen across 50 devices, in addition to the stressing results which will be discussed in 3.3.1, it was decided to progress with the lower doping times and investigate differing annealing times.

Table 2.2: Best performing devices with various copper deposition times

CuCl dwell time [s]	Anneal time [s]	Voc [mV]	Jsc [mA/cm^2]	FF [%]	Eff [%]
360	360	846	26.8	72.6	16.3
360	360	852	27.6	70.0	16.4
300	360	850	26.0	72.3	16.0
300	360	842	26.7	74.2	16.6
240	360	812	25.3	75.4	16.0
240	360	847	25.2	73.6	15.7

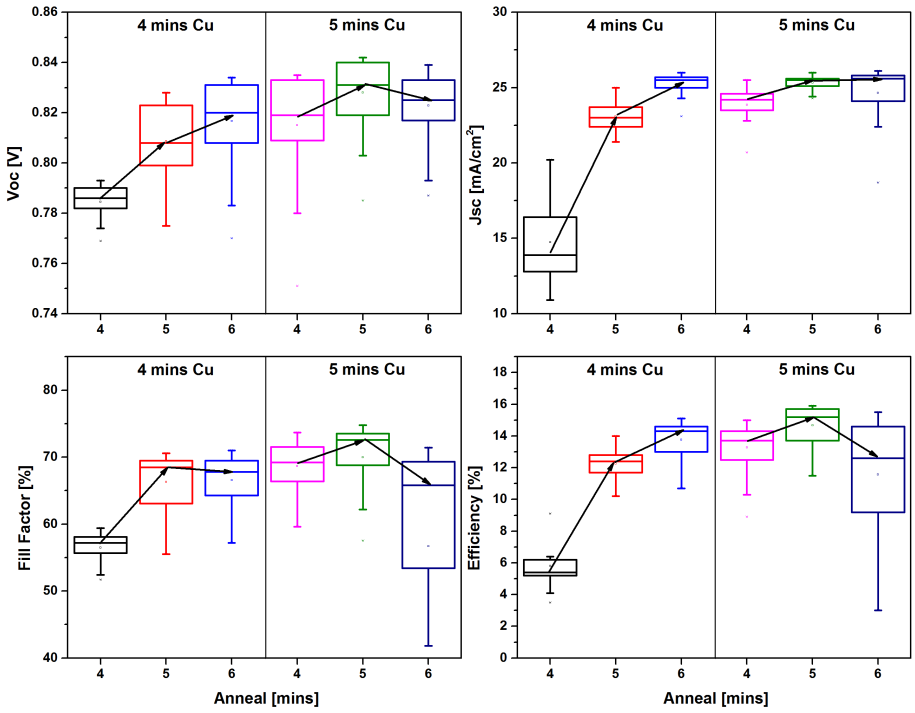

Figure 2.6: Main parameters for 25 devices per differing anneal time, demonstrating an increase in performance as annealing time is increased

Looking at figure 2.6 we note that in both cases, with 4 minutes or 5 minutes of copper doping, there is a major initial boost in performance when going from 4 minutes anneal time to 5 minutes anneal. However, as we move from 5 minutes anneal time to 6 minutes anneal time the gains are less pronounced, even decreasing in efficiency for those devices which received 5 minutes of

Table 2.3: Best performing devices with various copper anneal times

CuCl dwell time [s]	Anneal time [s]	Voc [mV]	Jsc [mA/cm^2]	FF [%]	Eff [%]
300	420	833	26.0	69.7	15.1
300	360	840	25.8	73.7	15.9
300	300	819	25.5	72.0	15.0
240	420	833	25.6	70.9	15.1
240	360	808	25.0	70.0	14.0
240	300	769	20.2	56.6	9.1

copper. This indicates that with a larger copper dosage, too large of an anneal time can drive the dopants further into the bulk and thus negligent in surface doping.

2.2.3 Sputtered metallic back contacts

This section will introduce a new method for depositing the back contact. Up to this point, all cells have used the typical colloidal nickle spray paint, as discussed in 1.3.4. Here we will diverge to using a sputtered metallic contact instead. In order to confirm that sputtered metallic contacts can achieve the same efficiencies as before, we begin by comparing the nickle paint contacts against sputtered nickle contacts. The specific target used was a Kurt J. Lesker nickle vanadium target (Ni:V), which is 93% Ni and 7% V by weight [42]. The V is introduced for sputtering purposes to create a nonferric target and is considered inconsequential to the sputtered Ni back contact. The Ni:V target is sputtered within the vacuum chamber described in Section 1.3.4.

Prior to deposition of the metallic back contact, plates were cut into sections, usually halves or fifths, such that the same absorber will receive differing back contacts to compare against. This is shown in Figure 2.7 where two halves of a plate received either sputtered Ni:V or Ni paint.

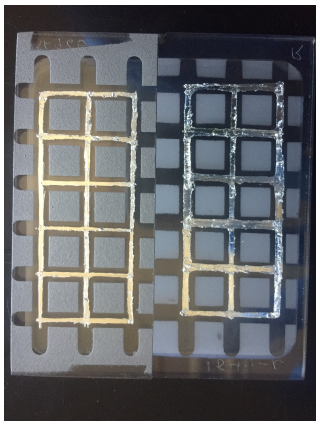

Figure 2.7: This plate was cut in half following deposition of the absorber layer, with the left half receiving a colloidal Ni based paint and the right half received sputtered Ni:V.

Initial JV measurements show that devices with Ni paint perform better, with an average efficiency of 10.92±2.90%. This is in comparison to an average efficiency of 8.56±3.01% for cells with sputtered Ni:V. The best performing device from three separate plates for each back contact is shown in Figure 2.8

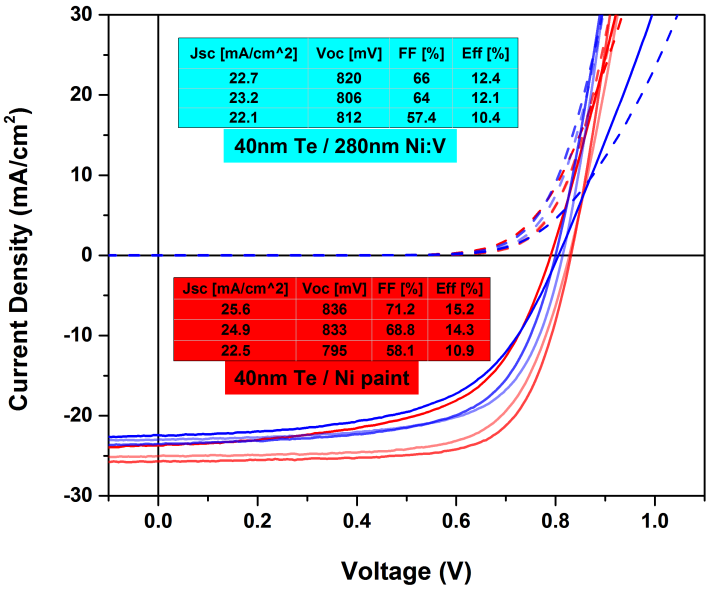

Figure 2.8: This graph displays JV curves for 6 device with either Ni paint (red) or sputtered Ni:V (blue) metallic back contacts.

EL imaging of these devices reveals the "softness" of the sputtered metals in comparison to the paint. This is seen from the edge damage done to cells during delineation with the sand blaster. Apart from the edge damage, these cells show a typical change in EL intensity with changing open circuit voltage.

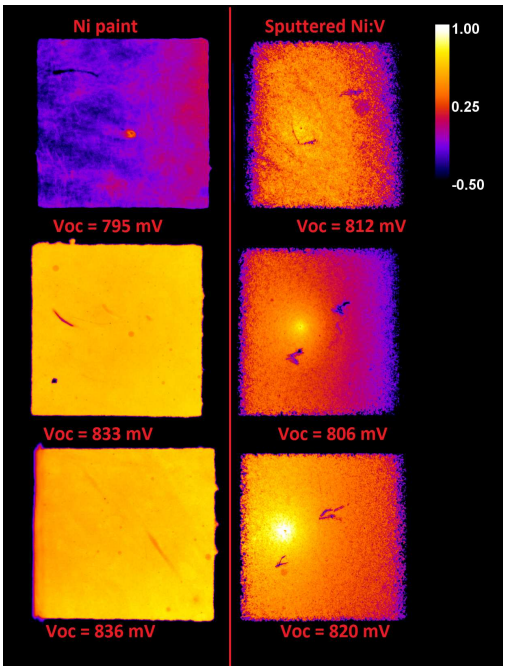

Figure 2.9: EL imaging shows the differance between identical absorbers with either a Ni paint or sputtered Ni:V metallic back contact. We see that a device with lower open circuit voltage has a decreased EL intensity regardless of the back contact.

These results indicate that a sputtered Ni:V metallic back contact can produce solar cells with appreciable conversion efficiencies. The next step involves looking at other sputtered metals to see how they effect performance as the band alignment is changed as discussed in Section 1.3.4. Given that the reported work function for Ni is between 4.1-5.0 eV, we expect that a sputtered Cr metallic back contact ought to have similar device efficiencies given a reported work function of 4.5 eV.

The initial Cr experiment was designed to fabricate identical absorbers across multiple plates which were cut in half prior to back electrode deposition to elucidate changes due to differing materials at the back surface. Plates were fabricated with the typical front contact and absorber design as discussed in earlier sections with a 5 minute copper doping and 5 minute copper anneal

followed by the deposition of 40nm of tellurium at the back surface. Plates were then cut in half, with one half receiving the colloidal Ni based paint solution as described in 1.3.4 while the other half received a sputter coat of 250nm thick chromium as shown in Figure 2.10.

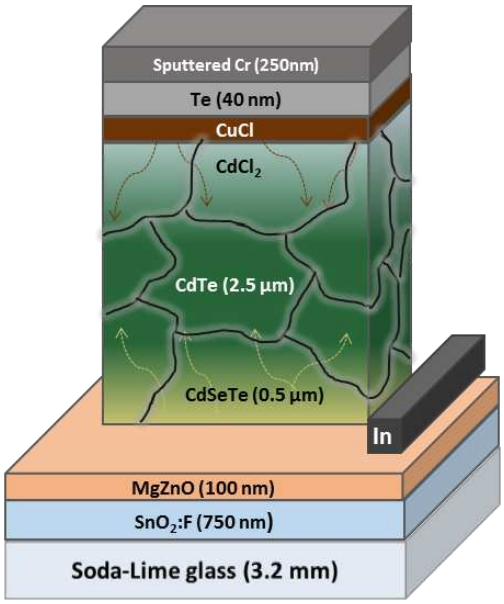

Figure 2.10: Schematic of the devices structure for cells fabricated at CSU that have a sputtered Cr metallic back contact

The initial JV, as measured within 24hrs of fabrication, is presented below for the 3 main plates with performance parameters listed in the table following

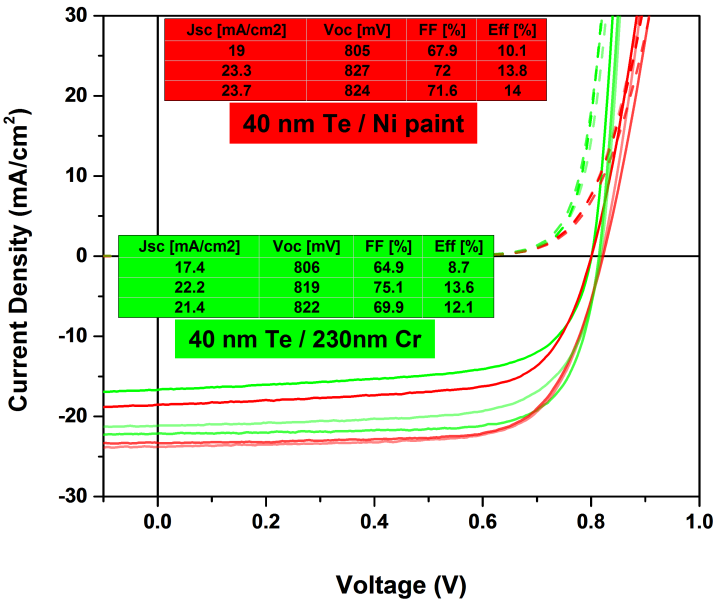

Figure 2.11: Initial JV curves for plates which are split in half and received either the colloidal Ni based spray paint (red lines) or received sputtered Cr (green lines). Ni tends to have better short circuit currents, but worse fill factors, demonstrating an increased series resistance.

Initial parameters show all plates having greater efficiency with paint contacts, primarily due to gains in Jsc which overcompensate for lower fill factors in most cases. On average the devices with Ni paint have an efficiency of 13.4±2.75% while the Cr sputtered devices have an average efficiency of 10.7±2.36%. We also note that the open circuit voltage is mostly independent of the metallic back contact, with at most a 1% difference, however the EL images show a large difference between the two types of contacts. The main issue seen in EL imaging is a "hot spot" on the sputtered Cr contacts where contact is made.

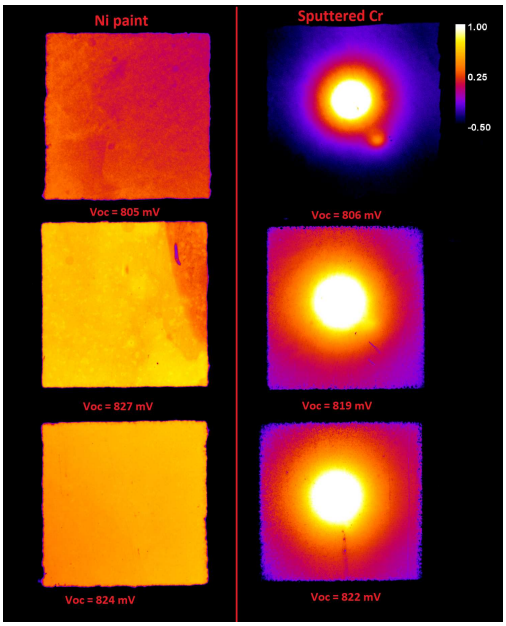

Figure 2.12: On the left are plates which have a colloidal Ni spray paint metallic back contact, plates on the right contain a sputtered cr metallic back contact. Although the open circuit voltages are comparable, we see the devices with Cr tend to have much lower intensity and demonstrate a "hotspot" where contact is made.

These results indicate that we are able to achieve reasonable efficiencies with devices which contain a sputtered Cr back contact in comparison to our typical structure. We will further discuss these cells in Section 3.3.2 where we will demonstrate that the sputtered Cr contacts tend to be more stable over time than those containing the Ni paint.

2.2.4 NiO as a buffer

Theoretical work has shown that in order to achieve > 25% efficient devices we will require minority carrier lifetimes (τ_e) > 25ns, a Front Surface Recombination Velocity (FSRV) <1E5 cm/s, and a CdTe free hole density (p_{CdTe}) > 2E16 cm^{-3} [43]. These models assumed that the back surface had flat band conditions however, with Back Surface Recombination Velocities (BSRV) on the same order as the front, 1x10^5 cm/s. This is not actually the case however, where back barrier heights have been calculated with a traditional ZnTe contact as between 0.3 and 0.6 eV and investigations in various buffer layers have shown barriers ranging from 0.15 - 0.3 eV [44–47].

Nickle oxide (NiO) has been used in the PV industry recently as a hole transporting layer for organic and perovskite based PV [48–50], indicating it's potential ability to transporting holes within thin film CdTe as well. Indeed, NiO has been explored within thin-film CdTe, where x-ray photoelectron spectroscopy (XPS) measurements demonstrated a valance band offset (VBO) of 0.52 eV between the CdTe and NiO layers, which leads to a calculated conduction band offset (CBO) of 2.68 eV, as shown in figure 2.13 [44]. This band structures allows NiO to act as an electron reflector layer in the back contact similar to the role that ZnTe has played in the past, while creating no barrier to hole transport. The electron-reflector is a property brought on by the presence of a back-surface-field (BSF) which reflects photo-generated electrons back into the CdTe bulk to prevent recombination at the back contact.

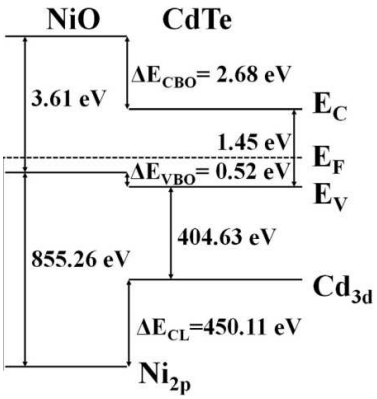

Figure 2.13: The band structure for the intrefacebetween CdTe and NiO as determined by X-ray photoelectron spectroscopy (XPS) [44].

Based on this research, NiO was selected as a metallic oxide buffer layer to be investigated. Initial analysis on the sputtered films has indicated that a 5nm thick layer is appropriate for our structures. Fabrication of CdTe solar cells was performed by the usual methodologies explored above, with NiO layers deposited following the absorber deposition. Following the deposition of NiO, the copper dopant was applied, which is able to diffuse through the thin buffer layer in order to dope our CdTe layer. In order to determine the affect of differing back contacts, while minimizing the possibility of differences between plate fabrications, each plate was divided into 5

strips, each receiving a different back contact treatment. The devices structures will be referred to in this section as Te/Ni (40nm Te/colloidal Ni paint), Te/Ni:V (20nm Te/280 nm sputtered Ni:V), and NiO/Ni:V (5 nm sputtered NiO/280 nm sputtered Ni:V). The remaining two back contact structures were both intended to evaluate ITO as a back contact for bifacial cells, and will not be presented here.

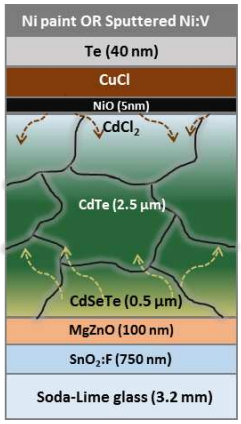

Figure 2.14: This graphic shows the structure for cells containing a NiO layer following the passivized CdTe surface with either the colloidal Ni based paint or a sputtered Ni:V layer.

JV curves for the top two cells for each back contact configuration are presented in Figure 2.15.

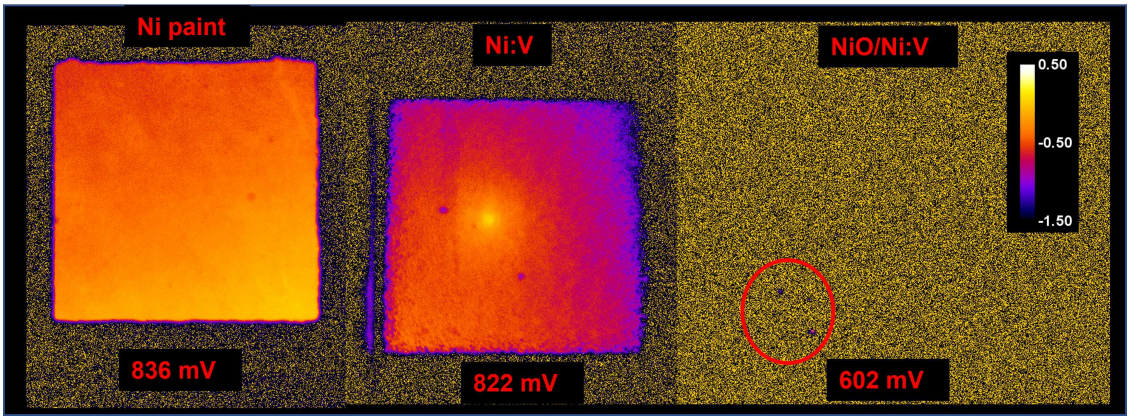

Figure 2.16: Differing EL images on three identical absorbers with differing back contacts. From left to right we have Ni paint, sputtered Ni, and NiO/sputtered Ni. Note the absence in illumination for the NiO containing cell, with small spots indicated by the red circle.

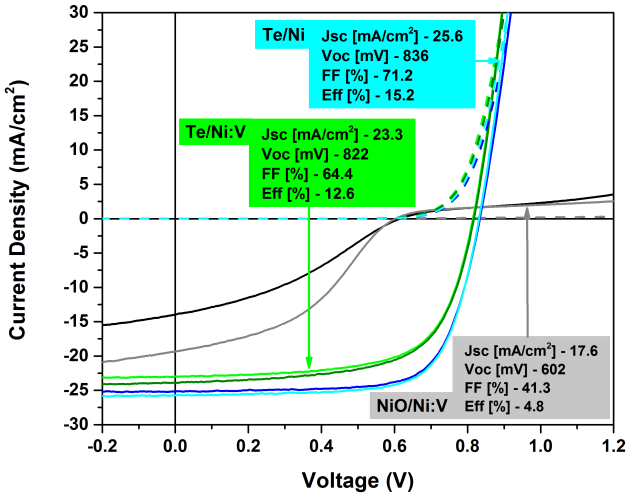

Figure 2.15: JV curves for two top performing devices for each back contact structure. It is evident from the curve that there is a back contact barrier causing rollover for NiO cells.

It is obvious from the JV curves presented in figure 2.15 that the cells containing a NiO buffer are experiencing roll over in forward bias with a very small saturation current.. The implications of this rollover are that a very large back barrier is present in devices which contain the NiO buffer layer.

The EL images show a clear difference between Te/Ni and Te/Ni:V cells and demonstrates the high resistance in NiO/Ni:V cells with a lack of luminescence. EL images of Te/Ni display a high uniformity across the surface, while Te/Ni:V tends to have a lower luminescence intensity as well as less uniformity, with an intensity gradiant present across the surface. Additionally, edge damage from delineation is obvious from the EL images. We also note the hot spot on the sputtered Ni:V cells, likely due to large through-conductivity in the sputtered metal.

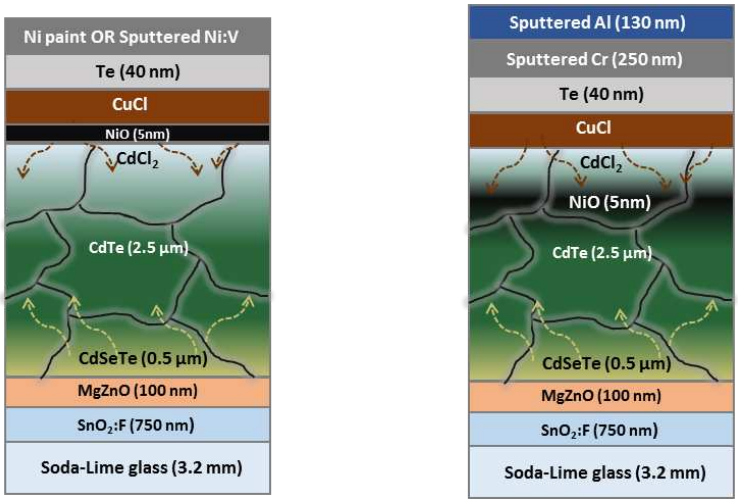

Figure 2.17: This graphic displays the differences in cell structure for devices with NiO. Left image is NiO deposited after passivation with Ni or Ni:V, resulting in rollover. Right image is NiO deposited before passivation with Cr Al bilayer, resulting in well behaved device.

Following these results indicating the presence of a back barrier when NiO is present led us to try and reduce the presence of the back barrier by introducing the $CdCl_2$ passivation processes following the NiO buffer as opposed to prior. These cells also contained a sputtered metallic bilayer of Cr+Al. Typically $CdCl_2$ is only introduced to the CdTe free surface; here we break the vacuum and deposit a 5nm thick layer of NiO before returning plates for $CdCl_2$ passivation in the ARDS. On the first attempt of this fabrication, it was noted that the $CdCl_2$ haze was not uniform across the surface, shown in Figure 2.18 resulting in similar device performance as before. This is evidence that the $CdCl_2$ passivation treatment is necessary after deposition of the oxide layer, not just after the absorber deposition.

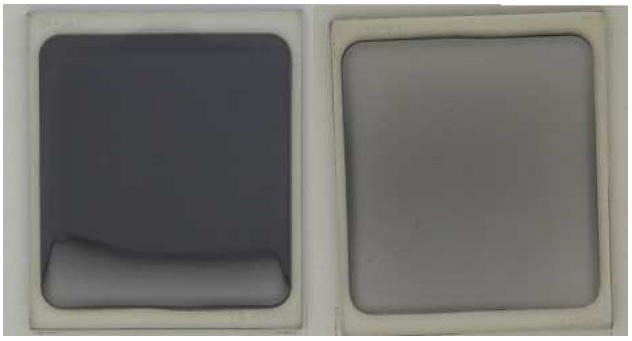

Figure 2.18: On the left is an example image of a plate with poor $CdCl_2$ haze, indication that the surface was not passivized. On the right is an example image with good $CdCl_2$ haze, demonstrating passivation of the entire surface.

Performing passivation after oxide deposition turned out to be fruitful, with the rollover effect completely removed as shown in Figure 2.19.

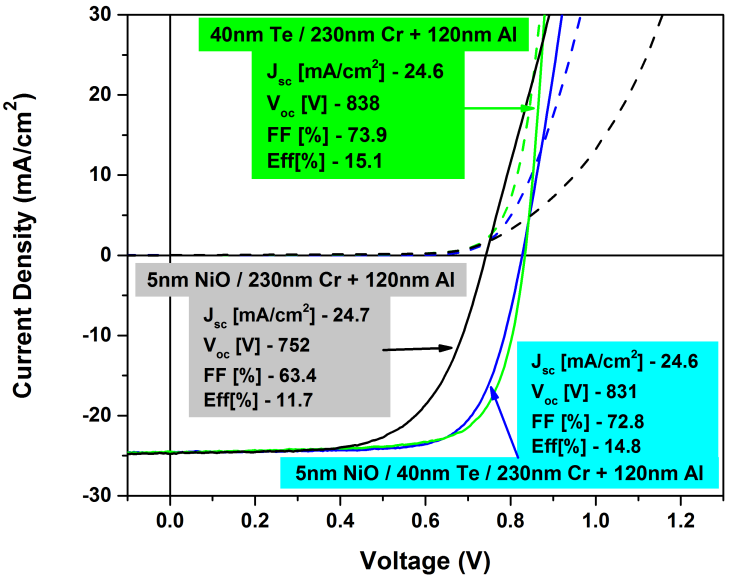

Figure 2.19: JV curves for cells containing a metallic bilayer back contact with and without NiO, with and without a Te buffer layer.

In addition to removing the back barrier by passivation of the NiO free surface, we attempted to determine the effect of removing the Te layer which is used to enhance p-type conductivity of

CdTe. As expected, the main result in removing the Te layer is a loss in open circuit voltage, as is shown in Figure 2.20.

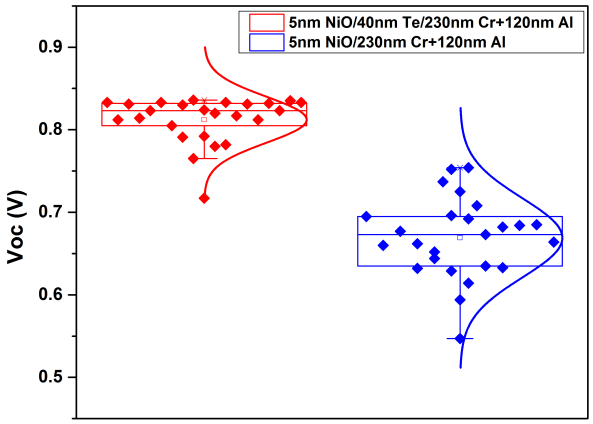

Figure 2.20: This graph shows the differance in open circuit voltage for those cells which have a NiO layer with with or without the Te back buffer, demonstrating increase Voc for those with Te.

These results confirm that NiO can be incorporated into CSU's main CdTe structure with average efficiency of 12.9±1.80%. Further EL imaging demonstrates luminosity similar to cells without the NiO buffer as shown in Figure 2.21.

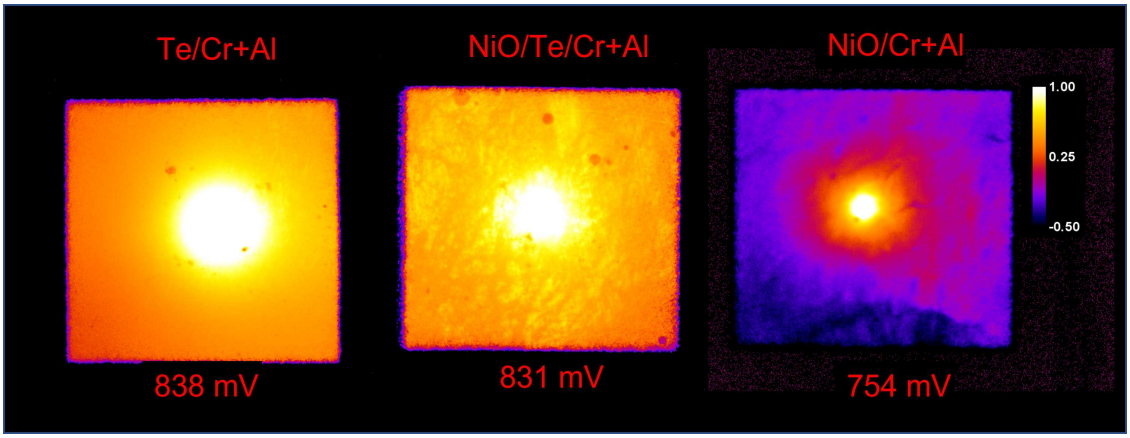

Figure 2.21: From left to right, we have our baseline structure with Cr+Al back contact, NiO with a Te buffer layer, and NiO without a Te buffer layer. The lack of luminosity for the last cell is in line with a reduction in open circuit voltage by 100mV.

Chapter 3

Stability of thin-film CdTe

In this chapter we will analyze how changes within PV devices over time and under various conditions impact performance and stability. The stability of photovoltaic devices is influenced by changing properties of constitute materials over time under and under various conditions, with perfectly stable devices having virtually no deviation from their initial performance. Understanding the factors which influence this stability and how it changes over time are imperative to fabricating nd maintaining PV devices for decades, however the underlying mechanism which drive stability changes are difficult to elucidate. Fundamental materials science tells us that drift and diffusion will be the main factors to change over time, in addition to possible phase changes due to extreme temperature changes or moisture ingress. However, due to the multiple complex factors which contribute to overall degradation, it is difficult to prescribe any certain process to a specific degradation route, be it migration of Cu in the absorber bulk, evolution of point defects from fabrication, or the formation of acceptor/donor complexes.

We will begin by going over the basic kinetics of degradation, with a focus on the drift and diffusion of carges/dopants. We will then examine the stability of various devices fabricated by the author under both ambient and ALTing conditions. Throughout this section, ambient conditions will be refereed to as those devices which are stored inside a desiccator at room temperature and with no illumination. ALTing conditions will be given in each relevant section.

3.1 Kinetics of degradation

The most fundamental properties which influence a PV device to change over time are atom/ionic drift and diffusion, even when in an ambient condition. Drift occurs due to forces from the built-in fields at junctions, while diffusion occurs as impurities influence local fields. These are both influenced by elevated temperatures, applied biases, and incident illumination.

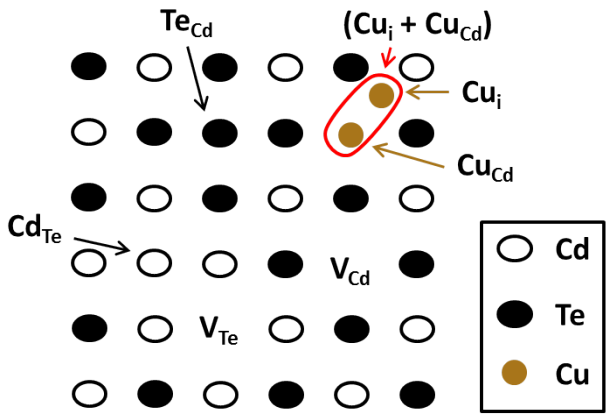

Figure 3.1: This figure depicts a schematics of typical defects found within the CdTe lattice when doped with Cu. The re circle represents the formation fo the neutral complex of (Cu$_i$ + Cu$_{Cd}$. Note that this figure does not represent the true 3D, zincblende, structure of CdTe.

3.1.1 Diffusion

Diffusion is a natural properties of materials governed by concentration gradients. Diffusion is modeled as a flux of particles from high concentraion to that of low concentration until equilibrium is established and is given by Fick's Law:

$$J_{x,diff} = -D_x \frac{dc}{dx} \tag{3.1}$$

where c is the concentration of given impurity and D$_x$ is known as the diffusion coefficient. The diffusion coefficint is given by the temperature dependent Arrhenius expression:

$$D_x = D_0 e^{\left(\frac{-E_x}{kT}\right)} \tag{3.2}$$

where E$_x$ is the activation energy of given defect and D$_0$ is the maximum diffusion coefficient.

Diffusion is characterized by two primary mechanisms: jumping of vacancies and migrating through interstitials. In vacancy hoping, a defect simply moves into an unoccupied lattice space adjacent to it. Interstitial migration occurs as a defect moves between interstitial states.

3.1.2 Drift

Charged ions are influenced by their total concentration and the presence of electric fields. The drift of concentration f(c) is given by

$$J_{x,drift} = q\frac{D_x}{kT}f(c) \tag{3.3}$$

where q is the charge of the defect and D_x is again the diffusion coefficient

3.1.3 Interaction between defects and charges

The complex movements of defects and charges within CdTe promote interactions which lead to changes in the electronic states of the bulk material. These changes can lead to deep defect states which increase recombination rates and end up altering the basic materials properties due to interstitial and substitution defects. In addition to the defect interactions, there are considerable problems associated with grain boundaries within polycrystalline films, where those grains tend to act as charge transport boundaries [51].

As discussed in Section 1.3.4, Cu is a commonly used dopant within CdTe to improve current collection, incerase the built-in potential, and improve the conductivity of the back surface. When introduced to the back surfafe, Cu can form donors (Cu_i), acceptors (Cu_{Cd}) and neutral complexes (Cu_i^+ - Cu_{Cd}^-) [39]. Cu has a large diffusion coefficient in CdTe (D=3 x10^{-12} cm^2/s [52]) which causes Cu to migrate from the back surface towards the main junction. Free Cu ions can form from the decomposition of complexes under stress, where highly conductive p-type Cd_2Te is reduced to CuTe while liberating free Cu atoms. These free Cu ions are then driven by field-assisted diffusion along grain boundaries. This is expressed through the equation below:

$$Cu_2Te \rightarrow CuTe + Cu^{++} + 2e^- \tag{3.4}$$

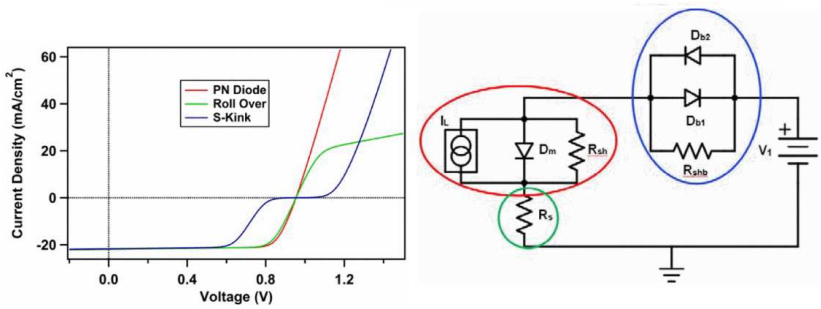

Figure 3.2: These two figures represent the distortions seen in JV curves and their equivalent circuit components which cause such distortions. The main PV diode is shown in red. The series resistance component in green accounts for general increases in resistance as well as the origin of forward bias rollover. The back diode component, with two diodes anti-parallel to each other, accounts for the formation of s-kinks.

3.1.4 Distortions to the J-V curve

Over time the J-V curves display distortions due to alterations of the chemical and electrical state fo the semiconductors within the device structure. Typical distortions seen and discussed in this work at increased series resistance, forward bias rollover, and power quadrant s-kinking. In this section we will review the current understanding of how these distortions form and discuss ways to mitigate them.

3.1.5 Forward bias rollover

Rollover is characterized by a saturation in the current collection when the solar cell is at large foward bias ($V > V_{oc}$). This is typiucally caused due to Schottky barrier formation at the back surface, which is modeled by the addition of second diode, (D_{b1}) into the typical PV equivalent circuit [36, 53]. This secondary diode represents the interface between CdTe and the back surface, whereas the main diode (D_m) represents the interface between CdTe and the front surface. In our case these represent the CdTe/metal interface and the CdTe/MZO interface respectively.

3.1.6 Power quadrant S-kinking

Unlike rollover, s-kinking is characterized by a premature increase in current flow at low bias ($V < V_{oc}$), followed by a reduction in current flwo around the open circuit voltage, and then a

resumptions in current flow for high bias ($V > V_{oc}$). This is modeled by the addition of a parallel diode (D_{b2}) with opposite polarity to that of D_{b1} [54]. This model allows for current flow at low voltage biases ($V < V_{oc}$), decreases the current flow near open circuit conditions ($V \approx V_{oc}$), and then allows current flow to resume at some bias greater than open circuit condition ($V > V_{oc}$). Similar to rollover, s-kinking is believed to be a result of an energy barrier within the bulk.

3.2 Accelerated Lifetime Testing

Accelerated Lifetime Testing (ALTing) is a commonly used methodology throughout engineering to determine the long-term stability of equipment under various loads and stresses, eventually elucidating the actual lifetimes of said equipment. Within the PV community, ALTing has been used to help suppliers frame warranties and manufacturers in determining best practices for device fabrication. Specifically within thin-film CdTe, a myriad of ALTing experiments has shown that there are three essential degradation mechanisms: the formation of a blocking contact, increased junction recombination, and increased dark resistivity

This section will discuss the process of ALTing for solar cells. We will begin with examining the advantages of ALTing, as well as the disadvantages and what cannot be confidently determined from such. We will then review the equipment used at CSU for ALTing and the work the author did in restoring the equipment back to functionality.

Following this introduction to ALTing and how it is done at CSU, results of various ALTing experiments will be

3.2.1 CSU Stress System

The ALT system at CSU, also known as the elevated-temperature stress system, was designed to provide precise and independent temperature and illumination control within a compact footprint [55]. The main body is a Fisher Scientific Isotemp 500 series oven with a 1.7 cubic foot capacity and a temperature range of up to 210 C. The oven has been modified to allow illumination by four LED arrays, Bridgelux 30G10K0L, each of which is mounted to a heatsink and cooling fan to

prevent from overheating, housed on top of the oven. The temperature set point and lights on/off are controlled via LabView software, which triggers a relay to provide power to the oven or LED arrays given the settings provided.

3.2.2 Troubleshooting the Stress System

In order to begin working with the Stress System, some modifications had to be made. Both the oven and the array of LEDs are powered on through a relay which is triggered by the user via LabView, thus the relay was by-passed during testing as to be able to troubleshot without need for the software. Initial tests showed the oven would turn on properly and heat up to the desired temperatures for each setting as desginated in the user manual. However, the LED array would not turn on, and subsequent investigations proved that two of four LEDs were shorted.

With all electrical systems tested, the oven and LED array were wired back into the relay and their response was tested through LabView, with the result being that all systems turned on properly, albeit with only two of four LEDs. The oven was then left to sit overnight to reach a steady state and confirm that all instruments were functioning properly at elevated temperatures and for an extended duration.

To determine the temperature at which our solar cells reside at while inside the oven, a representative superstrate glass was modified to incorporate thermocouples as shown in Figure 3.3. This glass slide was set into the stress oven while it was off, and the teperature was recorded every 5 minutes as the oven warmed up, with the lights on, until the set temperature was reached, after which the temperatures was recorded over the course of 3 hours until the glass reached a steady state.

Future improvements to the sytem remain to be made, and include replacing the back LEDs to further flood the area with light, improving the cooling mechanisms for the LED array and relay system, rewiring and reconfigure the interior airflow fans, and making quality of life improvements to the Automated Stress System LabView UI.

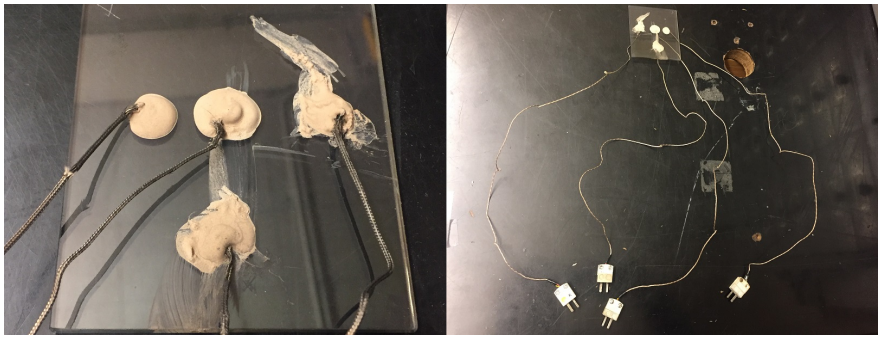

Figure 3.3: Holes were drilled into TEC10 glass and thermocouples were sealed in with thermal cement. These thermocouples were measured as the oven was warming up and while at steady state.

Time [mins]	Air temperature [C]	Glass temperature [C]			Time [mins]	Air temperature [C]	Glass temperature [C]		
2	25	23	23	23.5	25	79	58.5	53.8	52.5
			25					61.6	
5	33	28	27	26.5	30	80	58	52.2	51
			28					59.7	
10	45	39.8	38.2	37	60	80	57.2	52.7	52.2
			40.7					60.2	
15	60	46.2	44	43.7	150	80	62.6	59.7	60
			48.7					67.5	
20	71	54.7	50.5	48.8	225	80	63.4	61.4	61.1
			56.5					69.1	

Figure 3.4: This table shows the temperature of a sample glass slide within the ALT system exposed to stressing conditions. Temperatures are organized to correspond to each thermocouple showed in Figure 3.3. The glass reaches a steady state roughly 10 °C less than the air temperature.

3.3 Results of ALTing

In this section we will review the results of various ALTing experiments. All deivces presented here were fabricated and analyzed by the author. Devices are typically analyzed within 24 hours of fabrication, followed by storage in a desiccator (polyethylene box with air-tight silicon ring) in the dark at room temperature. As there is no illumination and no elevated temperature during this ambient storage phase, any changes within the materials will most likely be due to ionic drift due to internal fields or ionic diffusion due to concentration gradients.

3.3.1 3 μm absorbers with various Cu dopings

Stressing devices under elevated temperatures, with various amounts of copper, as defined by their deposition time, and annealed under various conditions, helps to understand not only the role that copper is playing in device performance, but also the optimal mechanisms for depositing Cu as a dopant. As discussed in section 1.3.4 copper is highly mobile in CdTe and is suspected to play various roles in the stability, or instability, in thin-film CdTe. Devices fabricated with various amounts of copper were initially discussed in section 2.2.2 with the top devices parameters shown in table 2.2. Following initial characterization, plates were cut into two pieces, one part to go into the oven for ALTing and the other part to act as a control in ambient conditions.

Devices for stressing were put into the ALT oven at 65 °C under constant illumination, with JV and EL conducted after 70 and 253 hours of stress. Control devices were also measured at the same time. It is clearly seen from the first measurements at 70 hours that there is a decrease in stability for cells containing greater Cu doping, as seen in figures 3.5 and 3.6.

The graphs of efficiency over time demonstrates six devices with roughly equivalent initial performance (Average 16.0 $\pm$ 0.2 %) with the devices containing the most Cu having peak performance. This trend reversed within the first 70 hours of stressing, as the device with the least copper demonstrated a 3% ambient and 29% stressed relative efficiency loss, 5 minute Cu devices showing 19% ambient and 43% stress relative efficiency losses and 6 minute devices showing the greatest

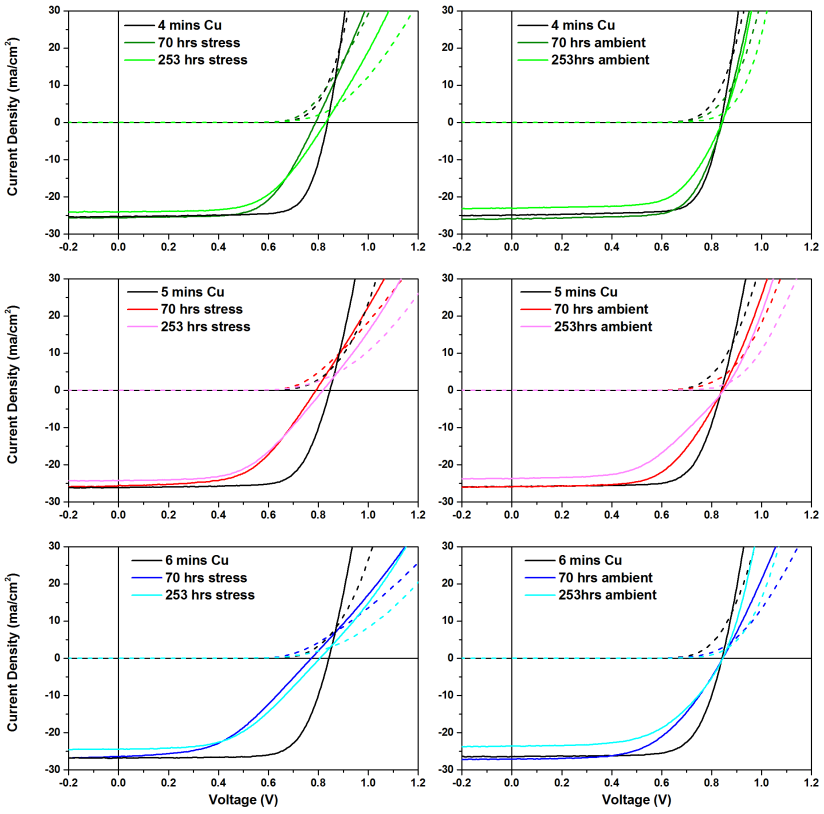

Figure 3.5: Devices subjected to ALTing are displayed on the left, with controls left in ambient conditions displayed on the right.

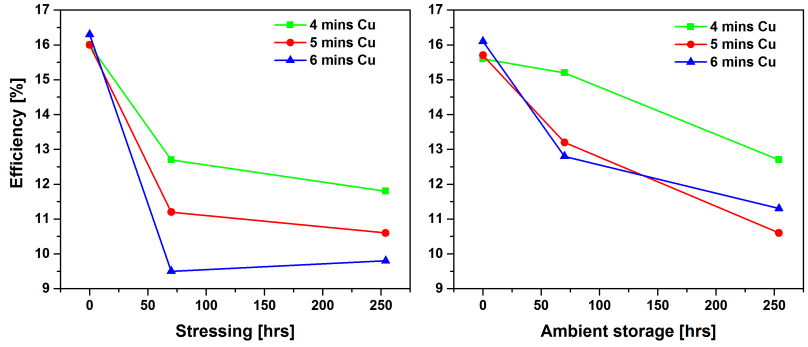

Figure 3.6: These graphs demonstrate how efficiency changes over time with devices under stress and those stored in ambient conditions. Note the inversion of performance between initial measurements and 70 hours.

losses at 26% ambient and 72% stress relative efficiency losses. These results are all displayed within the tables of figure 3.7.

With the ambient control group, we note the stability of the open circuit voltage, consistent with our understanding of degradation kinetics such that there should be no significant changes in carrier concentrations in these short times. The main factor leading to performance losses was fill-factor degradation, which is consistent at roughly 10% loss over 70 hrs for each minute extra of Cu doping. This seems to continue at a slower pace over the next 180 hours, albeit our 6-minute Cu device being an outlier in gaining back some of it's fill factor during that time.

For devices under stress, the open circuit voltage is unstable, first dropping in intensity after 70 hours, then recovering partially as the cell build up in series resistance. An increase in series resistance is the main JV distortion seen in these devices, with the control group also beginning to display signs of resistance buildup, which is more extreme for larger Cu doping times. This is indicative of the formation of a back contact barrier, which manifests quickest with more Cu and is experienced regardless of ambient or stressing conditions.

Device Description	Jsc [mA/cm^2]	Voc [V]	FF [%]	Eff [%]
4 mins Cu	25.3	0.841	75.4	16
70hrs stress	25.6	0.794	62.9	12.7
253hrs stress	24	0.834	59	11.8
Total %change	-5%	-1%	-28%	-36%
5 mins Cu	26	0.85	72.3	16
70hrs stress	25.8	0.795	55.4	11.2
253hrs stress	24.3	0.823	53.5	10.6
Total %change	-7%	-3%	-35%	-51%
6 mins Cu	26.8	0.846	72.6	16.3
70hrs stress	26.7	0.774	46.3	9.5
253hrs stress	24.5	0.812	49.7	9.8
Total %change	-9%	-4%	-46%	-66%

Device Description	Jsc [mA/cm^2]	Voc [V]	FF [%]	Eff [%]
4 mins Cu	25	0.839	75.1	15.6
70hrs ambient	25.9	0.848	69.8	15.2
253hrs ambeint	23	0.846	65.6	12.7
Total %change	-9%	1%	-14%	-23%
5 mins Cu	25.8	0.841	72.5	15.7
70hrs ambient	25.8	0.844	60.5	13.2
253hrs ambeint	23.6	0.852	52.6	10.6
Total %change	-9%	1%	-38%	-48%
6 mins Cu	26.4	0.845	72.5	**16.1**
70hrs ambient	27.1	0.848	55.8	12.8
253hrs ambeint	23.6	0.849	56.6	11.3
Total %change	-12%	0%	-28%	-42%

Figure 3.7: This table displays performance parameters as measured by JV for devices with various Cu doping times held under stress. Initial measurements are listed first, followed by the 70hr and 253hrs measurements. Percent differences between each step are listed to the right of each parameter, with overall percent differences listed below. Percent differences are all conditionally formatted such that gains performances are shaded green, then yellowing as performance losses are shaded red. Note the large losses following 70hrs stressing, with relatively mild losses, if not gains, achieved during the following 180hrs of stress.

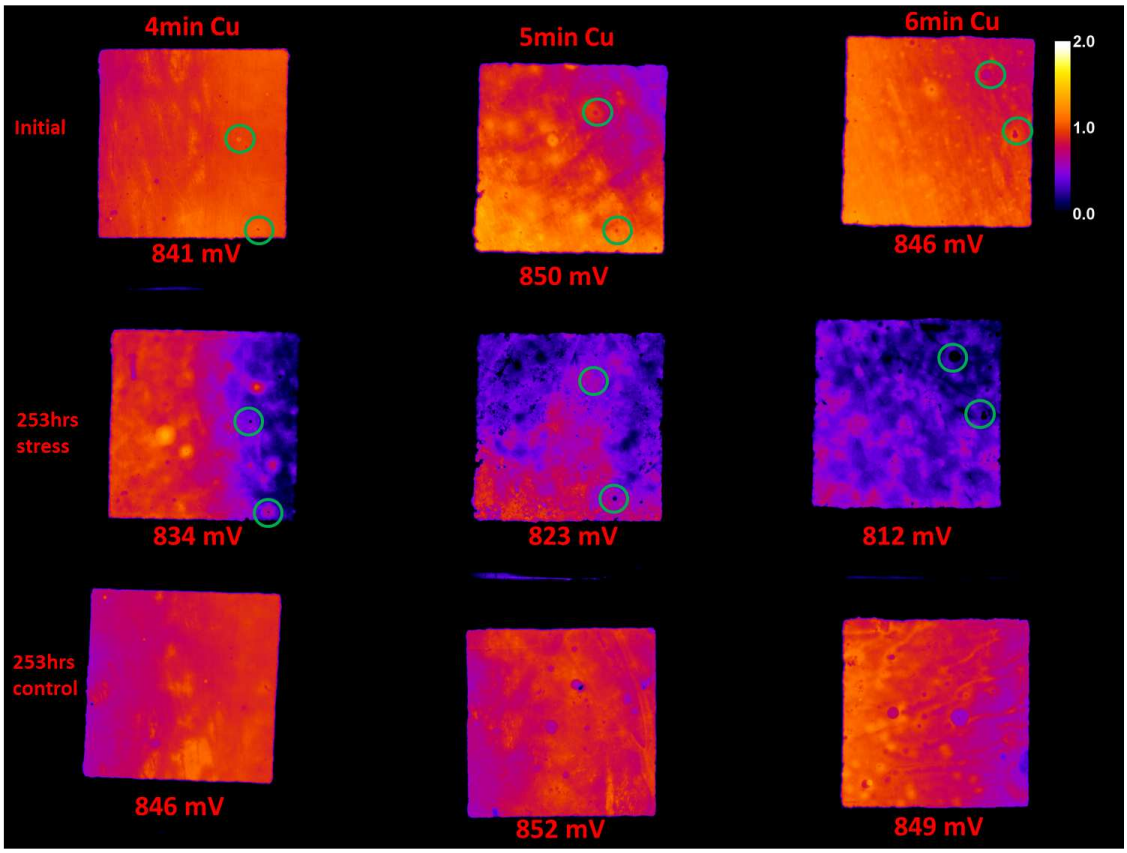

Figure 3.8: EL images for devices with differing amounts of Cu doping. Certain features from the initial images have been highlighted and shown again in the stressed images, demonstrating the formation of pinholes and shunts during ALTing. The bottom row contains control devices which were not stressed.

These changes were also seen in EL imaging, where devices initially emitted a uniform intensity spectrum across their surface independent of Cu doping, where both 4 and 6 minutes showed greater uniformity than 5 minutes. However, following 253 hours of stressing there is a noticeable difference in the uniformity of emitted intensity across the surfaces for highly doped devices. The open circuit voltages follow trend with EL image quality as well, with an 11-mV loss for each extra minute of Cu doping after 253 hours of stress.

Control devices left in ambient conditions were also imaged at the same time to determine what EL characteristics are induced through ALTing. These control devices display a slight non-uniformity in their emission profiles, although their open-circuit voltages remain in the same regime of those initial devices, demonstrating a reasonable stability.

3.3.2 3-μm absorbers with Ni paint or sputtered chromium

As discussed in section Section 2.2.3, this experiment was concerned with discerning differences experienced between identical absorbers with differing back contacts, namely either Ni based paint or sputtered Cr. Device fabrication was terminated prior to the final back contact, but after the Cu and Te depositions. Plates were cut in half and received Ni based paint on one half and sputtered Cr on the other half, similar to what is shown in Figure 2.8

Figure 3.9 is an example of the meta-stability of sputtered Cr back contacts in comparison to those with Ni paint under ambient conditions for 19 days. All cells with Ni paint demonstrated an unstable fill-factor, with at the very least an 8% loss and at most an 18% loss. Meanwhile, devices containing sputtered Cr had at most a 6% loss in fill factor, with all three devices increasing their short circuit current and open circuit voltage. The changes with the Ni paint are primarily due to increasing series resistance, which tends to also increase the open-circuit voltage a small amount, leading to at least a 1% gain in Voc for each cell. However, these gains in Voc are overshadowed by the large losses in fill factors for those devices with Ni paint. This leads to all three Cr devices gaining between 1% - 7% efficiency over 19 days of ambient storage, while devices containing Ni paint all lost between 10% - 44% efficiency. This is all shown in the tables of figure Figure 3.10.

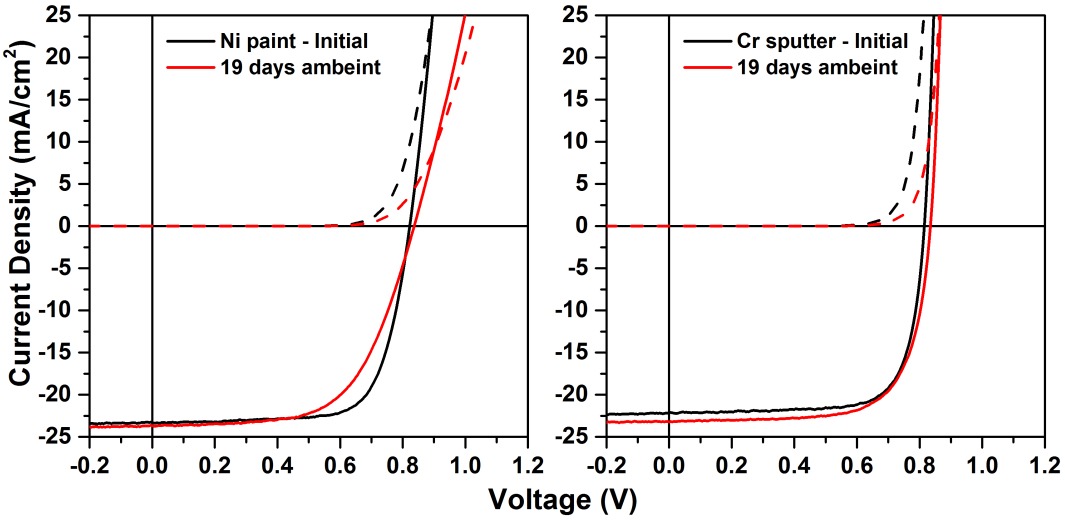

Figure 3.9: Example of stability of sputtered metal contacts under ambient conditions for 19 days. Paint devices tend to display increasing series resistance over time.

Ni paint				
ID	Jsc [mA/cm^2]	Voc [V]	FF [%]	Eff [%]
1872-4L-E2	19	0.805	67.9	10.1
19 days ambient	14.6	0.817	62.9	7
19 days % diff	**-30%**	**1%**	**-8%**	**-44%**
1872-5R-C5	23.3	0.827	72	13.8
19 days ambient	23.5	0.843	60.8	12
19 days % diff	**1%**	**2%**	**-18%**	**-15%**
1872-6L-E1	23.7	0.824	71.6	14
19 days ambient	23.7	0.841	63.9	12.7
19 days % diff	**0%**	**2%**	**-12%**	**-10%**
Sputtered Cr				
ID	Jsc [mA/cm^2]	Voc [V]	FF [%]	Eff [%]
1872-4R-E5	17.4	0.806	64.9	8.7
19 days ambient	18.7	0.829	63	9.4
19 days % diff	**7%**	**3%**	**-3%**	**7%**
1872-5L-C2	22.2	0.819	75.1	13.6
19 days ambient	23.3	0.841	71.1	13.8
19 days % diff	**5%**	**3%**	**-6%**	**1%**
1872-6R-E5	21.4	0.822	69.9	12.1
19 days ambient	22.4	0.842	68.4	12.8
19 days % diff	**4%**	**2%**	**-2%**	**5%**

Figure 3.10: The changes in main parameters over 19 days in ambient storage are tabulated for cells containing either Ni paint or sputtered cr metallic back contacts. Ni paint cells all decrease in efficiency while sputtered Cr cells all increase in efficiency.

Following 19 days in storage and after analysis was redone, with the 19 days ambient decay parameters now being considered the baseline for ALTing, each of these cells was placed into the ALTing oven. Stressing parameters for this experiment consisted of constant illumination under AM1.5 intensity at zero bias condition with zero humidity. The stressing temperature was increased from 50°C to 80°C over the course of 200 hours. Parameters for each stage of stressing are detailed in the below table

Stressing duration [Hrs]	Stressing temperature [C]	Illumination
0-44 [44]	50	AM1.5
44-114 [70]	60	AM1.5
114-125 [11]	70	AM1.5
125-200 [75]	80	AM1.5

Table 3.1: Stressing duration is listed with the specific hours during the 200 hour duration plates were subjected to specific temperatures, with the total hourly expose listed to the right of these.

As shown in Figure 3.11, starting from the ambient decay point, we generally see only minor J-V changes appearing in devices with a sputtered back contact as opposed to those devices with a paint back contact. Devices with paint back contacts display a growing series resistance, indication of a growing back contact barrier and one cells is beginning to demonstrate the formation of an s-kink and roll over effects.

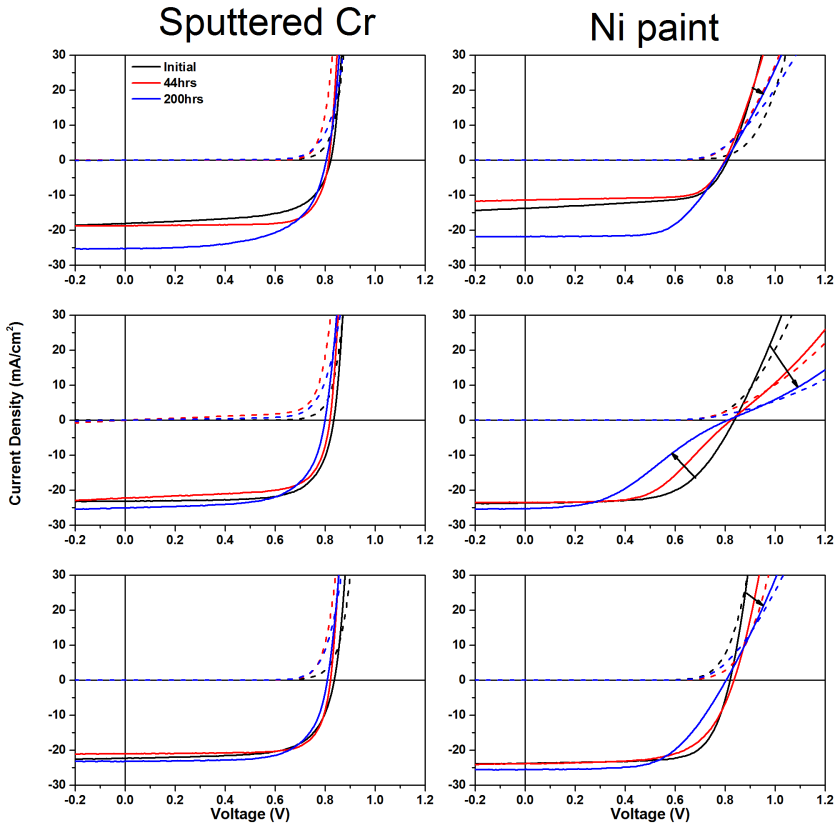

Figure 3.11: These curves represent 6 differant devices from 3 separate plates. Each half of a plate is grouped next to each other, such that each row shows devices from the same plate with identical absorbers. We see that for all three plates, devices containing Ni paint suffer from increasing series resistance, with one device developing an s-kink as well.

Sputtered Cr					Ni paint				
Stress [hrs]	Jsc [mA/cm^2]	Voc [V]	Fill Factor [%]	Efficiency [%]	Stress [hrs]	Jsc [mA/cm^2]	Voc [V]	Fill Factor [%]	Efficiency [%]
Initial	18.7	0.829	63	9.4	Initial	14.6	0.817	62.9	7
44	19.1	0.819	75.9	11.6	44	12.1	0.808	71.9	6.6
200	25.3	0.807	61	12.4	200	21.9	0.808	63.6	11.2
	26%	-3%	-3%	24%	Total % diff	33%	-1%	1%	38%
Initial	23.3	0.841	71.1	13.8	Initial	23.5	0.843	60.8	12
44	22.5	0.823	69.6	12.7	44	23.6	0.827	53.8	10.4
200	25.1	0.802	66.3	13.3	200	25.1	0.811	38.2	7.8
	7%	-5%	-7%	-4%	Total % diff	6%	-4%	-59%	-54%
Initial	22.4	0.842	68.4	12.8	Initial	23.7	0.841	63.9	12.7
44	21.2	0.826	76.4	13.2	44	24	0.824	69.4	13.6
200	23.3	0.811	70	13.1	200	25.6	0.806	59.8	12.2
	4%	-4%	2%	2%	Total % diff	7%	-4%	-7%	-4%

Figure 3.12: The percent differences for main parameters of devices under stress with either Ni paint or sputtered Cr metallic back contact.

From the changes in main parameters as presented in Figure 3.12 we see that after 200 hours of stressing, each group of devices had one cell with moderate gains in efficiency, Ni paint having a 38% overall gain and sputtered Cr a 24% overall gain. However, these large gains in efficiency can be accounted for by a 33% and 26% respective increase in short circuit current for both cells. Both groups also demonstrated a cell with an overall 4% loss in conversion efficiency.

This leaves one cell from each group, with the Ni paint cell having a 54% loss while the sputtered Cr cell shows a 2% gain in efficiency. This large difference can be accounted for by losses in fill factor for the Ni paint device, with both cells demonstrating similar changes in Jsc and Voc. Overall, devices with Ni paint lost an average of 7% efficiency while devices with sputtered Cr gained an average of 7% efficiency.

EL images reveal modest stability for the cells containing Ni paint and those with sputtered Cr. Cells with sputtered Cr show damage where contact was made and we see more damage on the 200 hour image as a result of additional measurements taken. Cells with sputtered Cr also have a hot spot which persists after ALTing. Each full plate which was cut in half is presented together, with histograms for each EL image given below each image.

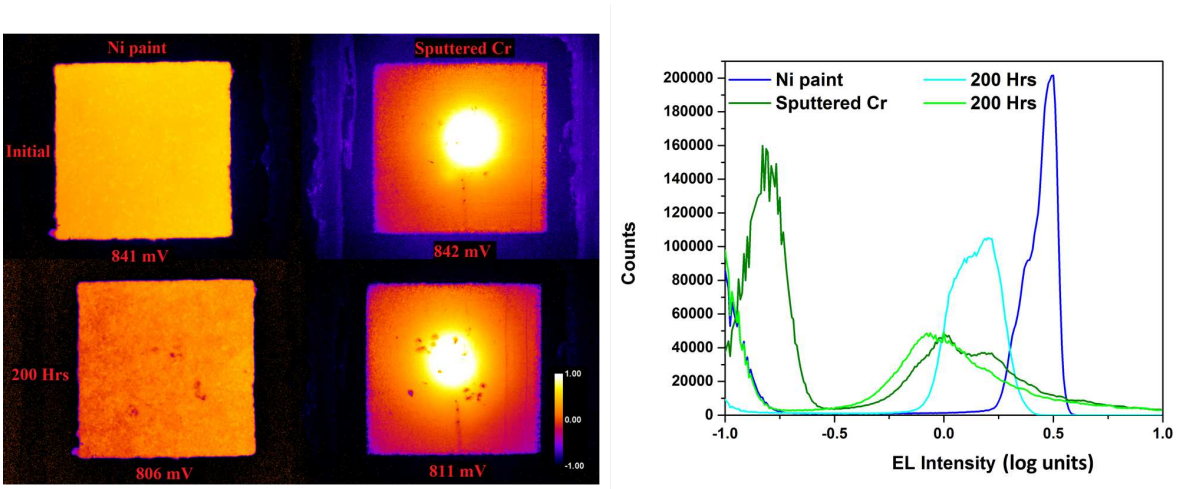

Figure 3.13: Ni paint EL shows stability despite this being the device which lost 54% relative efficiency over 200 hours. The drop in luminosity is consistent with such a loss in open circuit voltage. We again see evidence of the "softness" of the sputtered metals as more damage appears in the 200 hours image for sputtered Cr. However, the EL intensity bucks the trend with dropping open circuit voltage here.
Ni paint shows the brightest peak here, centered at 0.5. After 200 hours this peak shifts to about 0.2 and the entire curve drops in intensity.
Sputtered Cr shows good stability after 200 hours, with an initial broad peak around 0 and a slight shift down to -0.1 after 200 hours.

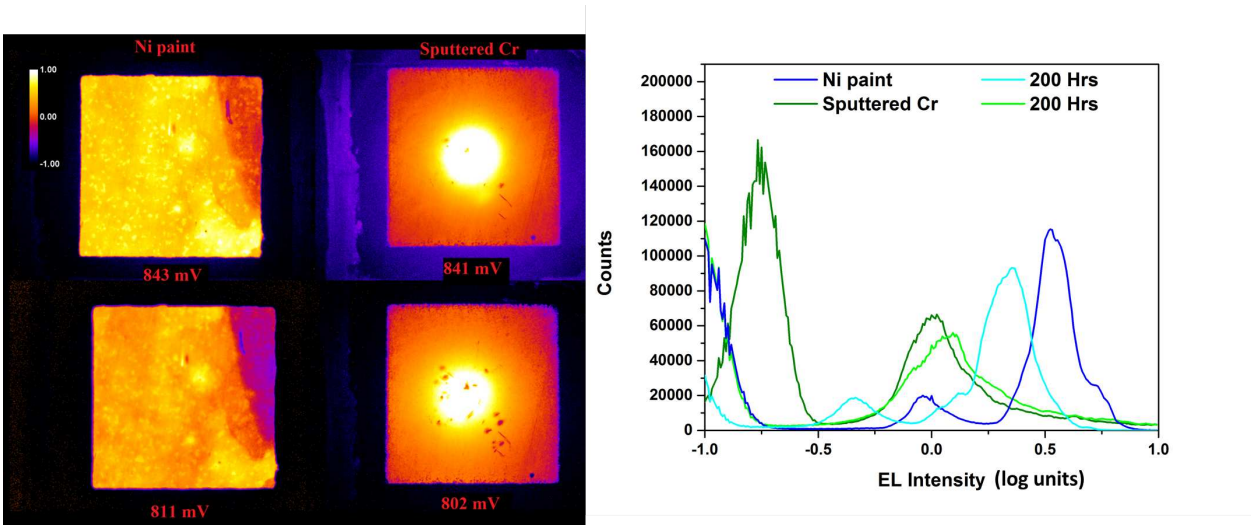

Figure 3.14: Ni paint again shows the freckling but with the freckled spots becoming less intense rather than more intense as in the first image. Sputtered cr displays the same types of damage as before, and again with stable intensity despite a drop in Voc.
For Ni paint we see a large main peak around 0.6 with a small secondary peak around 0. The secondary peak accounts for the dim spot at the top right of the EL image. After 200 hours this entire form is shifted down in intensity as expected with a drop in Voc.
Sputtered Cr again shows a less intense and broader peak centered around 0. After 200 hours the shape remains roughly the same, with the peak shifting up slightly despite the cell having a greater loss in open circuit voltage than its Ni paint counterpart.

Chapter 4

Conclusions and Future work

4.1 Conclusions

In this thesis we have shown that changes to the back contact structure of thin-film solar cells are able to replicate the results of our initial structure, even coming close to the highest efficiency with our most complex structure as shown in the table below.

Back Contact	Jsc [mA/cm2]	Voc [mV]	FF [%]	Eff [%]
40 nm Te/Ni paint	26.2	842	69.1	15.2
40 nm Te/230nm Cr + 120 nm Al	24.6	838	73.9	15.1
5nm NiO/40 nm Te/230nm Cr + 120 nm Al	24.6	831	72.8	14.8

Moreover, we have demonstrated that these changes provided for a more stable, albeit less robust solar cell at the end of the day. Devices with Ni paint tend to build up in series resistance over time, leading to an average of 7% loss in efficiency during stressing. The devices with sputtered contacts did no show this large increases in series resistance however, where they actually gained an average of 7% efficiency during stressing.

We also saw from EL imaging that those cells with sputtered contacts tended to retain their peak intensity, while those cells with Ni paint tended to see a downshift in their peak intensity over time. The robustness of paint contacts is seen in the EL imaging as additional scratches develop on the sputtered metals but not on the paint.

This experimental work has also confirmed that our work to bring the CSU stress system back to operational mode after over a year in idle was successful. The oven was able to operate at a steady state for hundreds of hours without any significant problems.

4.2 Future work

This thesis has presented initial results which are indicative of work to come. We would like to continue with stressing devices while incorporating a more well rounded suite of analysis techniques to better understand the underlying kinetic mechanics driving long term stability of solar cells.

We would like to make modifications to the CSU stress system to upgrade the lighting and cooling systems, as well as manufacturing a new mount to enable biasing under stressed conditions. We would also like to incorporate more factors into the stressing analysis, such as various biases applied to cells under stress and evaluating diffing environmental factors such as humidity and general exposure.

Additional back contacts are to be experimented with as well. We would like to look into Pt and Au contacts, differing metallic bilayers, and potential organic contacts. Additional oxide and buffer layers at the back contact will also be evaluated. We would also like to explore different methods of depositing Cu and Te at the back surface for increased conductivity and doping, hopefully with techniques which can be incorporated into industrial practices for a quicker and cheaper process.

Bibliography

[1] IEA. World energy balance overview.

[2] A. Priani S. L. Connors V. Masson-Delmotte, P. Zhai. Climate change 2021: The physical science basis: Contribution of working group 1 to the sixth assessment report of the intergovernmental panel on climate change. *Cambridge University Press*, 2021.

[3] US Energy Information Administration. Renewable energy explained, 2021.

[4] U.S. Energy Information Administration. August 2021 monthly energy review. 2021.

[5] Axion Power. Powering the entire wrold with solar: Surface area and panel requirements, 2021.

[6] Linda Capuano. U.s. energy information administration'sinternational energy outlook 2020, October 2020.

[7] S. Hegedus. Thin film solar modules: the low cost, high throughput and versatile alternative to si wafers. *Progress in Photovoltaics: Research and Applications*, 14(5):393–411, 2006.

[8] The Electrochemical Society. Semiconductor applications: From transistors to solar cells, 2021.

[9] Martin A. Green. *Solar cells: operating principles, technology, and system applications.* Englewood Cliffs, NJ, Prentice-Hall, Inc., 1982.

[10] S. M. Sze. *Physics of semiconductor devices*. Wiley-Interscience, Hoboken, N.J, 2007.

[11] Hitachi High-Tech. Properties of semiconductors.

[12] Tao Song. *Design Structures for High Efficiency Solar Cells*. PhD thesis, Colorado State University, 2015.

[13] Natarajan Pandiarajan, Ramabadran Ramaprabha, and Ranganath Muthu. Application of circuit model for photovoltaic energy conversion system. *International Journal of Photoenergy*, 2012:1–14, 2012.

[14] Utsho A Arefín, M. Razib, Md Shojib, and Baka BIllah. Characterization & analysis of iii-v multi-junction pv solar-cells. 01 2016.

[15] N F Mott. Note on the contact between a metal and an insulator or semiconductor. *Proceedings of the Cambridge Philisophical Society*, 34:568, 1938.

[16] H K Henisch. *Rectifying Semiconductor Contacts*. Clarendon, Oxford, 1957.

[17] Kwan Chi Kao. Charge carrier injection from electrical contacts. pages 327–380. Elsevier, 2004.

[18] A Luque. *Handbook of photovoltaic science and engineering*. Wiley, Chichester, West Sussex, U.K, 2011.

[19] Russell Geisthardt, Marko Topic, and James Sites. Status and potential of cdte solar-cell efficiency. *Photovoltaics, IEEE Journal of*, 5:1217–1221, 07 2015.

[20] Dietrich A. Jenny and Richard H. Bube. Semiconducting cadmium telluride. *Physical Review*, 96(5):1190–1191, dec 1954.

[21] D. De Nobel F. Kruger. *J. Electron*, pages 190–202, 1955.

[22] Xuehai Tan, Shou Peng, Chuanjun Zhang, Akash Saraf, Guogen Liu, Shenjiang Xia, Jingong Pan, Velappan Krishnakumar, Bastian Siepchen, Alan E. Delahoy, and Ken K. Chin. How to control the stoichiometry of cadmium telluride thin film for photovoltaic applications. *Journal of Renewable and Sustainable Energy*, 9(6):063505, nov 2017.

[23] Joseph J. Loferski. Theoretical considerations governing the choice of the optimum semiconductor for photovoltaic solar energy conversion. *Journal of Applied Physics*, 27(7):777–784, jul 1956.

[24] Kim Mitchell, Alan L. Fahrenbruch, and Richard H. Bube. Photovoltaic determination of optical-absorption coefficient in CdTe. *Journal of Applied Physics*, 48(2):829–830, feb 1977.

[25] Martin A. Green, Ewan D. Dunlop, Jochen Hohl-Ebinger, Masahiro Yoshita, Nikos Kopidakis, and Xiaojing Hao. Solar cell efficiency tables (version 58). *Progress in Photovoltaics: Research and Applications*, 29(7):657–667, jun 2021.

[26] Taesoo D. Lee and Abasifreke U. Ebong. A review of thin film solar cell technologies and challenges. *Renewable and Sustainable Energy Reviews*, 70:1286–1297, apr 2017.

[27] *Handbook of Photovoltaic Science and Engineering*. PAPERBACKSHOP UK IMPORT, March 2011.

[28] J.M. Kephart, J.W. McCamy, Z. Ma, A. Ganjoo, F.M. Alamgir, and W.S. Sampath. Band alignment of front contact layers for high-efficiency CdTe solar cells. 157:266–275, dec 2016.

[29] Elisa Artegiani, Mauro Leoncini, Marco Barbato, Matteo Meneghini, Gaudenzio Meneghesso, Marco Cavallini, and Alessandro Romeo. Analysis of magnesium zinc oxide layers for high efficiency CdTe devices. *Thin Solid Films*, 672:22–25, feb 2019.

[30] Amit H. Munshi, Jason M. Kephart, Ali Abbas, Tushar M. Shimpi, Kurt L. Barth, John M. Walls, and Walajabad S. Sampath. Polycrystalline CdTe photovoltaics with efficiency over 18% through improved absorber passivation and current collection. *Solar Energy Materials and Solar Cells*, 176:9–18, mar 2018.

[31] Francesco Bittau, Christos Potamialis, Mustafa Togay, Ali Abbas, Patrick J.M. Isherwood, Jake W. Bowers, and John M. Walls. Analysis and optimisation of the glass/TCO/MZO stack for thin film CdTe solar cells. *Solar Energy Materials and Solar Cells*, 187:15–22, dec 2018.

[32] Lokendra Kumar, Beer Pal Singh, Aparna Misra, S.C.K. Misra, and T.P. Sharma. Characterization of CdSexTe1-x sintered films for photovoltaic applications. *Physica B: Condensed Matter*, 363(1-4):102–109, jun 2005.

[33] Graham Lane Maxwell. Characterization and modeling of cdcl2 treated cdte/cds thin-film solar cells. Master's thesis, Colorado State University, 2010.

[34] Amit H. Munshi, Jason M. Kephart, Ali Abbas, Adam Danielson, Guillaume Gelinas, Jean-Nicolas Beaudry, Kurt L. Barth, John M. Walls, and Walajabad S. Sampath. Effect of CdCl2 passivation treatment on microstructure and performance of CdSeTe/CdTe thin-film photovoltaic devices. *Solar Energy Materials and Solar Cells*, 186:259–265, nov 2018.

[35] Thomas A. M. Fiducia, Kexue Li, Amit H. Munshi, Kurt Barth, Walajabad S. Sampath, Chris R. M. Grovenor, and John Michael Walls. Three-dimensional imaging of selenium and chlorine distributions in highly efficient selenium-graded cadmium telluride solar cells. *IEEE Journal of Photovoltaics*, 10(2):685–689, mar 2020.

[36] S.H. Demtsu and J.R. Sites. Effect of back-contact barrier on thin-film CdTe solar cells. *Thin Solid Films*, 510(1-2):320–324, jul 2006.

[37] J. Hölzl and F. K. Schulte. Work function of metals. pages 1–150. Springer Berlin Heidelberg, 1979.

[38] Elisa Artegiani, Jonathan D. Major, Huw Shiel, Vin Dhanak, Claudio Ferrari, and Alessandro Romeo. How the amount of copper influences the formation and stability of defects in CdTe solar cells. *Solar Energy Materials and Solar Cells*, 204:110228, jan 2020.

[39] C Corwine. Copper inclusion and migration from the back contact in CdTe solar cells. *Solar Energy Materials and Solar Cells*, mar 2004.

[40] MG Chemical. 841ar – super shield nickel conductive coating, 2021.

[41] Dirk C. Jordan, Sarah R. Kurtz, Kaitlyn VanSant, and Jeff Newmiller. Compendium of photovoltaic degradation rates. *Progress in Photovoltaics: Research and Applications*, 24(7):978–989, feb 2016.

[42] Kurt J. Lesker. Nickel vanadium (ni/v, 93/7 wt%) sputtering targets, 2021.

[43] A. Kanevce, M. O. Reese, T. M. Barnes, S. A. Jensen, and W. K. Metzger. The roles of carrier concentration and interface, bulk, and grain-boundary recombination for 25% efficient CdTe solar cells. *Journal of Applied Physics*, 121(21):214506, jun 2017.

[44] Di Xiao, Xun Li, Dongming Wang, Qiang Li, Kai Shen, and Deliang Wang. CdTe thin film solar cell with NiO as a back contact buffer layer. *Solar Energy Materials and Solar Cells*, 169:61–67, sep 2017.

[45] Colin A. Wolden, Ali Abbas, Jiaojiao Li, David R. Diercks, Daniel M. Meysing, Timothy R. Ohno, Joseph D. Beach, Teresa M. Barnes, and John M. Walls. The roles of ZnTe buffer layers on CdTe solar cell performance. *Solar Energy Materials and Solar Cells*, 147:203–210, apr 2016.

[46] Khagendra P. Bhandari, Prakash Koirala, Naba R. Paudel, Rajendra R. Khanal, Adam B. Phillips, Yanfa Yan, Robert W. Collins, Michael J. Heben, and Randy J. Ellingson. Iron pyrite nanocrystal film serves as a copper-free back contact for polycrystalline CdTe thin film solar cells. *Solar Energy Materials and Solar Cells*, 140:108–114, sep 2015.

[47] Tao Song, Andrew Moore, and James R. Sites. Te layer to reduce the CdTe back-contact barrier. *IEEE Journal of Photovoltaics*, 8(1):293–298, jan 2018.

[48] Seongrok Seo, Ik Jae Park, Myungjun Kim, Seonhee Lee, Changdeuck Bae, Hyun Suk Jung, Nam-Gyu Park, Jin Young Kim, and Hyunjung Shin. An ultra-thin, un-doped nio hole transporting layer of highly efficient (16.4*Nanoscale*, 8:11403–11412, 2016.

[49] Jae Woong Jung, Chu-Chen Chueh, and Alex K.-Y. Jen. A low-temperature, solution-processable, cu-doped nickel oxide hole-transporting layer via the combustion method for high-performance thin-film perovskite solar cells. *Advanced Materials*, 27(47):7874–7880, oct 2015.

[50] Jong H. Kim, Po-Wei Liang, Spencer T. Williams, Namchul Cho, Chu-Chen Chueh, Micah S. Glaz, David S. Ginger, and Alex K.-Y. Jen. High-performance and environmentally sta-

ble planar heterojunction perovskite solar cells based on a solution-processed copper-doped nickel oxide hole-transporting layer. *Advanced Materials*, 27(4):695–701, nov 2014.

[51] J. Perrenoud, L. Kranz, C. Gretener, F. Pianezzi, S. Nishiwaki, S. Buecheler, and A. N. Tiwari. A comprehensive picture of cu doping in CdTe solar cells. *Journal of Applied Physics*, 114(17):174505, nov 2013.

[52] Matteo Bertoncello, Fabio Casulli, Marco Barbato, Elisa Artegiani, Alessandro Romeo, Nicola Trivellin, Enrico Zanoni, Matteo Meneghini, and Gaudenzio Meneghesso. Influence of CdTe solar cell properties on stability at high temperatures. *Microelectronics Reliability*, 114:113847, nov 2020.

[53] T.J. McMahon and A.L. Fahrenbruch. Insights into the nonideal behavior of CdS/CdTe solar cells. In *Conference Record of the 28th IEEE PVSC*. IEEE, 2000.

[54] Paul J. Roland, Khagendra P. Bhandari, and Randy J. Ellingson. Electronic circuit model for evaluating s-kink distorted current-voltage curves. In *2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)*. IEEE, jun 2016.

[55] John Raguse, Russell Geisthardt, Jennifer Drayton, and James R. Sites. Compact accelerated life testing with expanded measurement suite. In *2014 IEEE 40th Photovoltaic Specialist Conference (PVSC)*. IEEE, jun 2014.